

‘

‘

. . .

“

68000”

“

”

6.0924, 6.0907, 6.0925

8

9.03.2004 .

2004

681.335.5(075)

2004 .

- . .
- . .

	“		”.	-
	-	()	
68000	()	6800		
	,	,	680 0,	-
	.	.		-
68230	68681	.		-

18 4 2003 .

- . .

- . .

70- XX . ” -
 ” (), .
 MC680X0 , () -
 (), () -
 MC68000. , ,
 , , ,
 ” -
 , . -
 , MC68000
 680X0, 683XX -
 , -
 () MC68000 MC680X0, -
 . -

1

MC68000. -
 (). -
 2 -
 MC68000. () -
 - , - -
 () MC68230 (/ - /) MC68681 (-
 / - /). -
 (-
 ,). ,
 (. 2.1), , ()
 8 ×8 , 16 ×8 , 32 ×8 , 64 ×8 .

2.1 –

	,	,	/ ;	/
1	32	96	1; 00, A↓ B↓	1
2	64	128	2; 00, A↑ B↑	2
3	16	48	1; 00, A↑ B↓	2
4	8	32	1; 00, A↓ B↑	1
5	64	192	1; 01, A↓ B↓	2
6	32	32	2; 01, A↑ B↑	2
7	16	16	2; 01, A↓ B↑	2
8	16	8	2; 01, A↑ B↓	2
9	64	64	2; 1x, A↓ B↓	2
10	96	96	2; 1x, A↑ B↑	2
11	32	128	1; 1x, A↓ B↓	1
12	128	128	2; 1x, A↑ B↑	2
13	128	192	1; x0, AB↑	1
14	8	24	1; x0, AB↓	1
15	8	8	1; x1, AB↑	1
16	8	16	1; x1, AB↑	2
17	8	64	1; 2, A↑	1
18	48	64	1; 2, A↓	1
19	16	32	1; 2, B↑	2
20	32	64	1; 2, B↓	2
21	4	24	1; 3, AB↑	1
22	24	64	1; 3, AB↓	1
23	48	96	1; 00, A↑	1
24	96	96	1; 01, A↓	2
25	32	128	1; 1x, A↑	1
26	16	96	1; 1x, B↑	1
27	32	16	2; x0, AB↓	1
28	48	128	1; x0, AB↑	1
<p style="text-align: center;">- ,</p> <p style="text-align: center;">- ,</p> <p style="text-align: center;">/ - /</p> <p style="text-align: center;">/ - /</p> <p style="text-align: center;">/ : 0 (00,01,1X); 1(X0,X1); 2; 3</p> <p style="text-align: center;">- 00 A↓, B↓; - A↑, B↑. , 00, A↓ B↑</p> <p style="text-align: center;">0: , - ;</p> <p style="text-align: center;">2, A↓ 2.</p>				

, , / / , -

/ -

3

4 (210×297), -

, , , -

- , :

()

1

2

2.1

2.2

2.3

2.4

2.5

3

4

- / ()

4

() 68000

- () -

- ,

[1].

68000 (. 4.1)

(68000

), (23... 1), (D₁₅...D₀), -

(), , , -

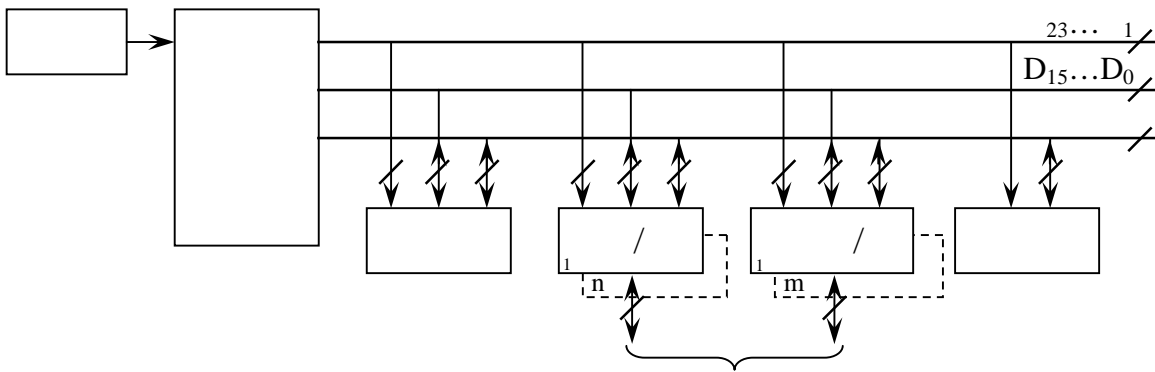
/

(), () -

68230 (

/) 68681 (

/ /);
 () . , , , -
 () . () -
 , / , / -
 () .
 () -



4.1 -

5

() .
 - () .
 [1].
 68000 (-
 86) . -
 , . -
 () , -
 [2].

23... 0 N5N4N3N2N1 0, -

N5 -

N5).

N4

N3N2N1 -

()

N3

N2

N1 (5... 1) -

5,

0 = 0

0 = 1 -

4... 1.

N3 (

),

5

/

68000

(),

0 = 1,

0 = 0.

32 = 10¹⁵.

14... 1 (N3N2N1),

16 = 2¹⁴ (14-

).

N4

2⁻¹ < m ≤ 2, m - = 2,

m = 3

16 15.

: 00 (N4 = 11

), 01 (), 10 (

N5 (23... 17)

N5 = 0000000.

() 000000000 14... 10, 000000001 14... 10.

() -

N4 10. N2

7 6 (), N3 -

14... 8,

N3 = 0000000.

N2 = 11

5, N2 = 00 / , N2 = 01 1- / , N2 = 10 -
 2- / .

0000.00001.0000.0000.1000.0001=010081

8- 0000 2-
 / 5 / ,
 5 .



[1],

5.1

68000 (CPU),

(GN)

68000 [2]

(), 16-

()

23-

().

Vcc GND (. 5.1)
 +5 .

23... 1

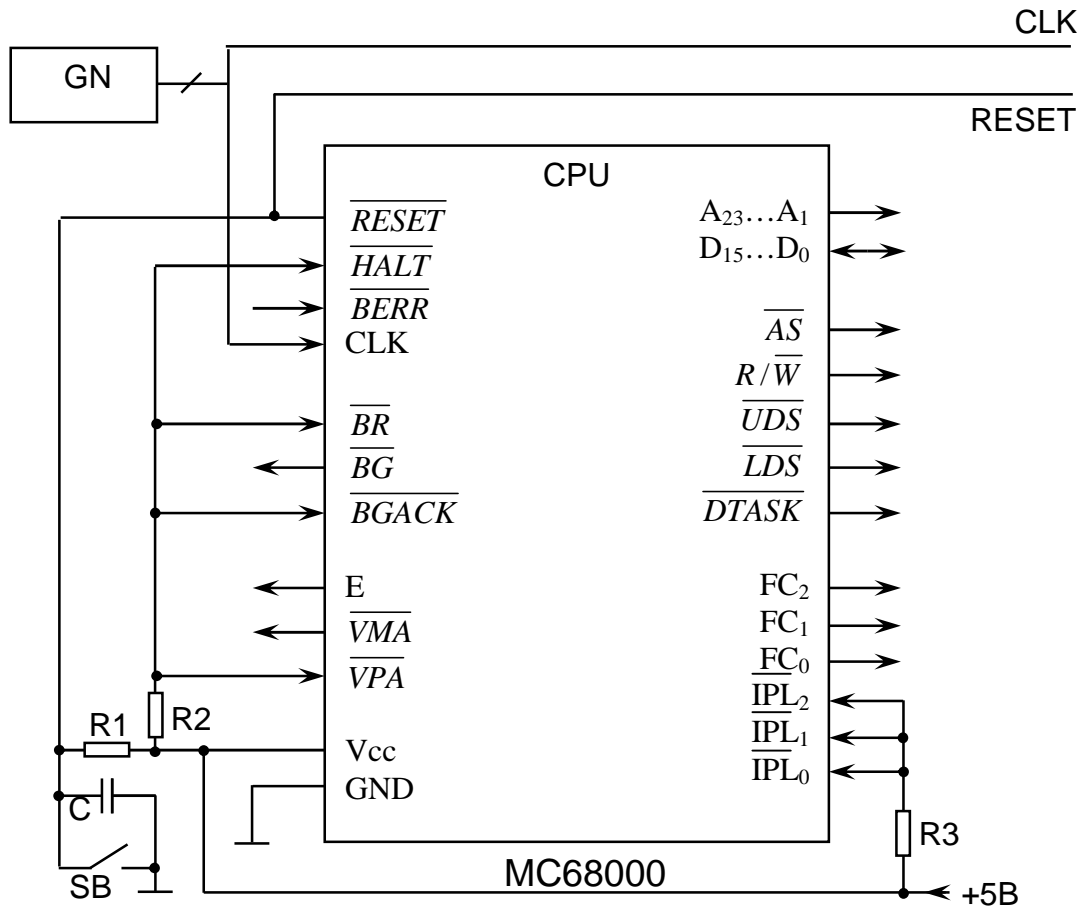
D₁₅...D₀

\overline{UDS} \overline{LDS} .

. CLK -

. CLK

. \overline{RESET} -



5.1 -

$\overline{RESET} = 0$

SR

S =

1 (\$000

),

0.

SSR

\$004 -

SR,

\overline{RESET}
SB

. 5.1.

$\overline{RESET} = 0$

RESET,

$\overline{HALT} = 0$ ()

23... 1, D15...D0

(),

$\overline{HALT} = 0$

$\overline{BERR} = 0$,

$\overline{RESET} = 0$

$$\overline{BERR} = 0$$

,

$$\overline{DTACK} = 0$$

,

$$\overline{AS} = 0$$

S₀ S₁

$$(5.2). \overline{R/\overline{W}} = 0$$

$$(\overline{R/\overline{W}} = 1;$$

$$\overline{LDS} = 0$$

$$\overline{UDS} = 0, \overline{LDS} = 0$$

$$\overline{UDS} = 1, \overline{LDS} = 0,$$

$$\overline{DTACK} = 0$$

$$\overline{UDS} = 0, \overline{LDS} = 1.$$

$$\overline{DTACK} = 1.$$

$$(\overline{DTACK} = 0)$$

$$(\overline{DTACK} = 1)$$

$$(\overline{BR} = 0)$$

$$\overline{BR} = 0,$$

$$\overline{BR} = 0,$$

$$D_{23...15}, D_{15...0}$$

$$\overline{BG} = 0$$

$$\overline{BGACK} = 0$$

$$\overline{BGACK} = 0,$$

$$(\overline{BR} = 1)$$

$$\overline{BGACK} = 1.$$

LK.

$$\overline{VMA} = 0,$$

$$\overline{VPA} = 0$$

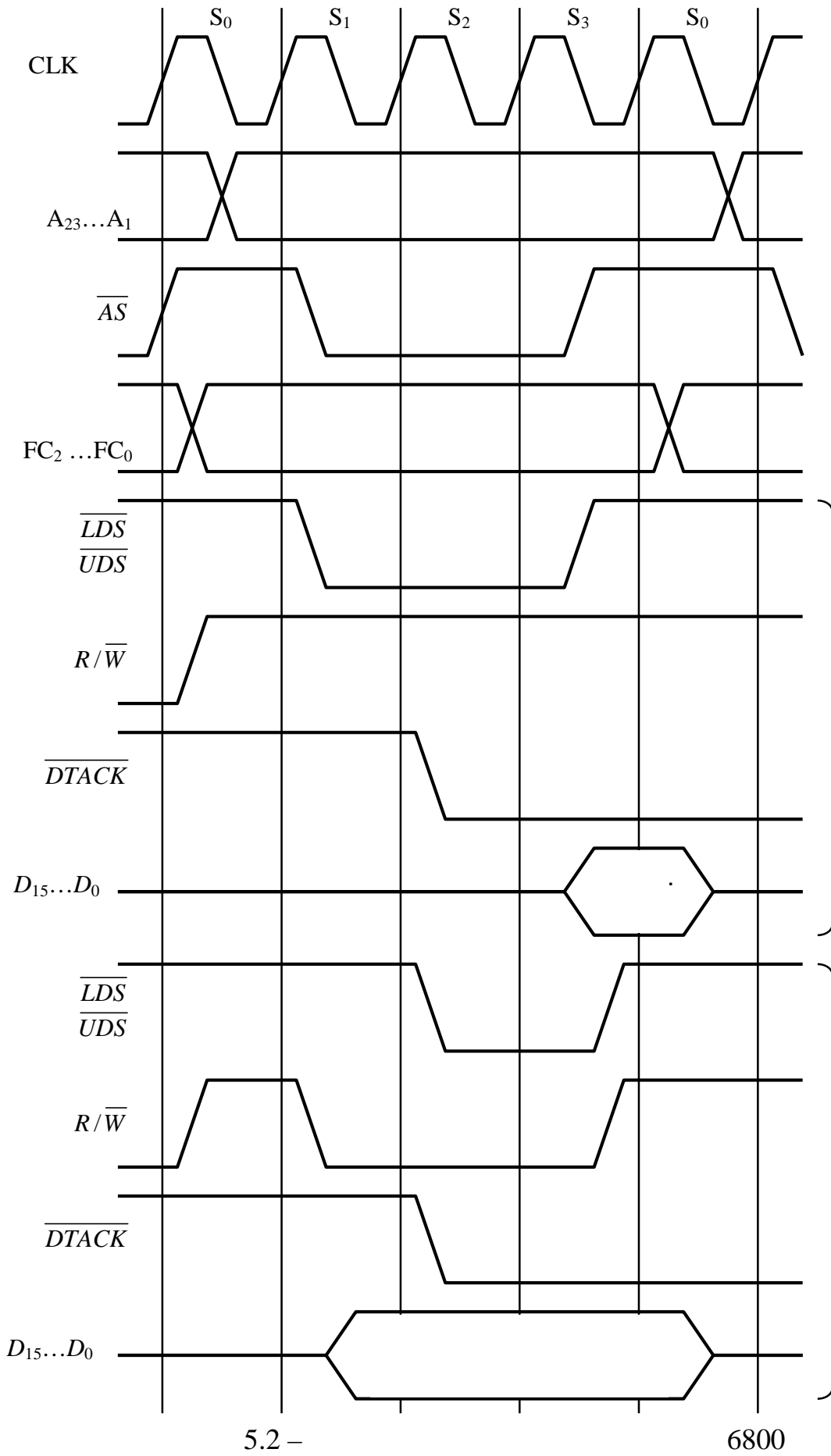
D_{23...15}

$$\overline{AS} = 0, \overline{R/\overline{W}} = 0$$

FC_{2...0}

FC_{2...0}

$$\overline{INTA} = 0$$



5.2 -

6800

IPL₂...IPL₀.

IPL₂...IPL₀,

111

5.1

R

+5

GN

5.2

()

5.3: A - N-

5.3.

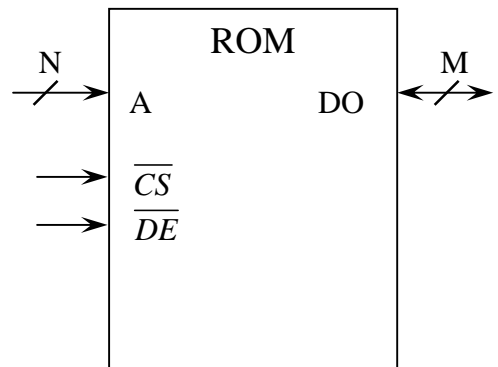
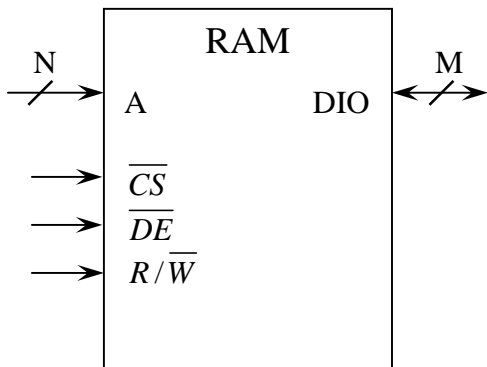
DIO -

CS -
R/W -

DIO -
DE -
DO -

N

, DIO DO.



5.3 -

:) - ,) -

2^n ($n = 1, 2, 3, 4, 5, 6$).

5.4

32

14... 1.

()

DC1.

DC1

N4 (16 15).

N4
). \overline{OE} ($S_1 \dots S_3$ (. 5.2))
 DC1 (DC₀, DC₁) \overline{CS}
 DC1₂
 DC1
 DC1₃.
 DC1₀ DC1₁
 (14... 1) DO DIO
 D_{7...D₀} ,
 - D_{14...D₈}.
 \overline{DE}
 $\overline{DE}_L R M$
 (), \overline{DE}
 $\overline{DE}_H R M$ “ ”
 \overline{DE}
 $\overline{DE}_L RAM$ $\overline{DE}_H RAM$.
 R/\overline{W}
 5.1, $\overline{DE}_H = 0 -$
 () ; $\overline{DE}_L = 0 -$
 () .

5.1 -

	\overline{UDS}	\overline{LDS}	R/\overline{W}	\overline{DE}		\overline{DE}		R/\overline{W}	
				\overline{DE}_H	\overline{DE}_L	\overline{DE}_H	\overline{DE}_L		
0	0	0	0	1	1	0	0	0	
1	0	0	1	0	0	0	0	1	,
2	0	1	0	1	1	0	1	0	
3	0	1	1	0	1	0	1	1	,
4	1	0	0	1	1	1	0	0	
5	1	0	1	1	0	1	0	1	,
6, 7	1	1	X	1	1	1	1	X	

.5.1.

5.3

- 2...4.

DC2. DC2

N2

(\overline{OE}),

DC1.

DC2

\overline{CS} () .

10 ($A_7A_6 = 11 -$

).

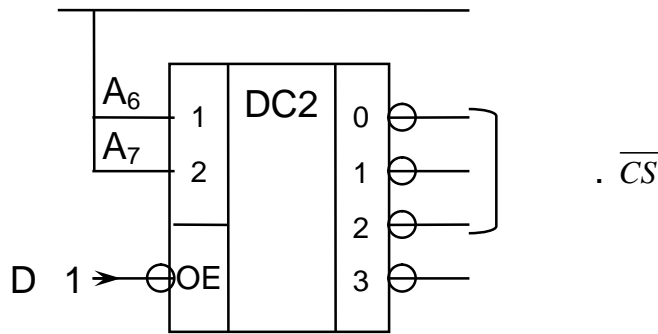
D 2

N2

$A_7A_6: 00, 01,$

. 5.5.

DC2



5.5 -

D 2

5.3.1 /

(. 5.6)

68230 [3].

R/\overline{W} ,

\overline{RESET}

68000, $CLK - GN.$

\overline{DTACK}

\overline{DTACK}

DC1₀ DC1₁,

D_{7...D₀},

RS_{5...RS1}

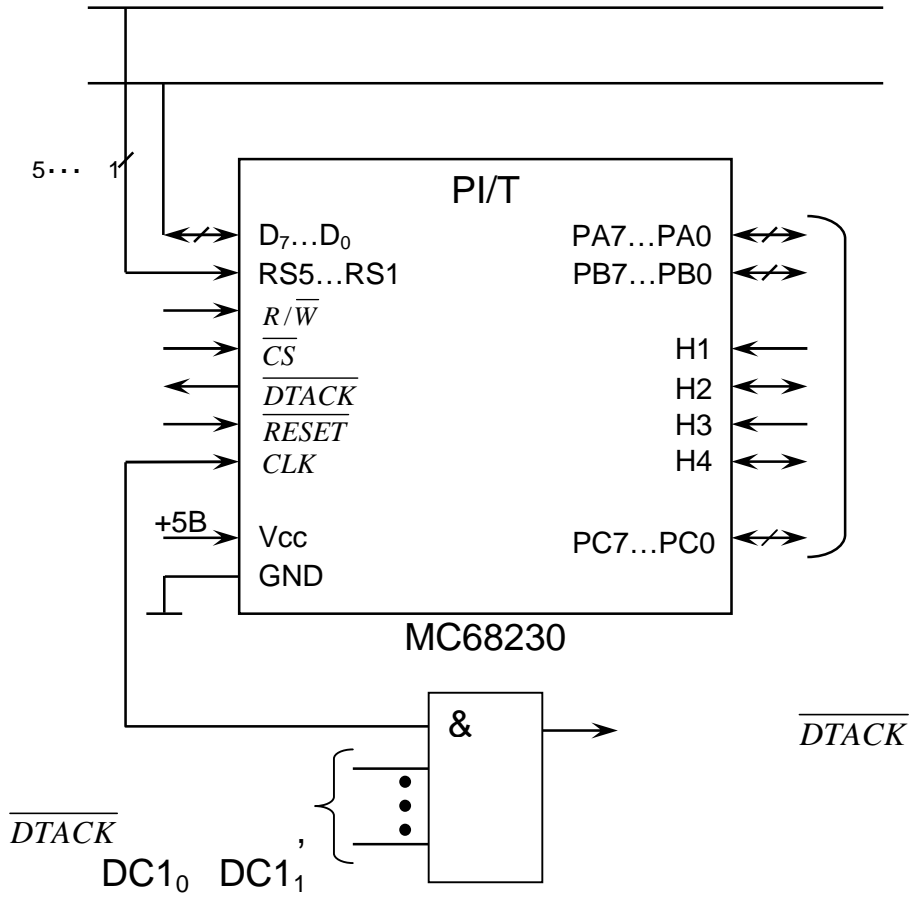
5... 1.

68230

4... 1,

7... 0

7... 0 ()



5.6 –

7... 0 ()

68230.

5.3.2

68681 [4]

IACK

(. 5.7)

D7...D0

A4...A1

RS4...RS1,

68681

R/W, RESET

, 1/CLK – GN,

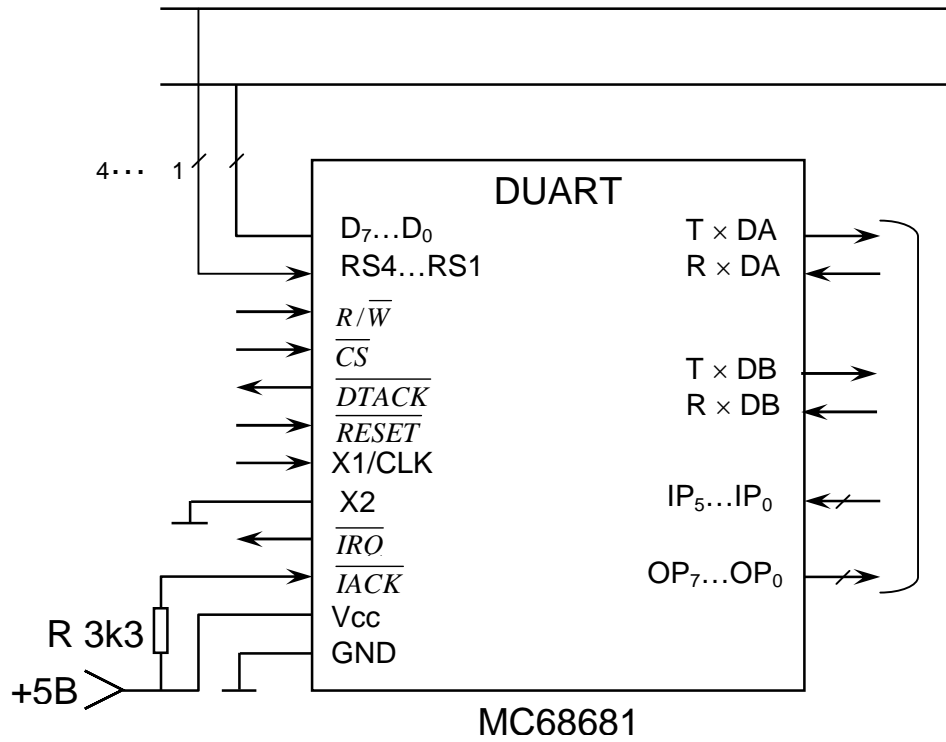
X2

68681

[4].

/ ,

-



5.7 – 68681 /

\overline{DTACK} (. . 5.6) .
 \overline{CS} DC2. \overline{IRQ} (-
)) . \overline{IACK}
 () . T x DA T x DB
 / , R x DA R x DB -

5... 0 -
7... 0 -

, / -
 / , / / 68861. -
 , , / -

5.4

- ()
 \overline{BERR} . (. 5.8)
 N5, N3 5 , -

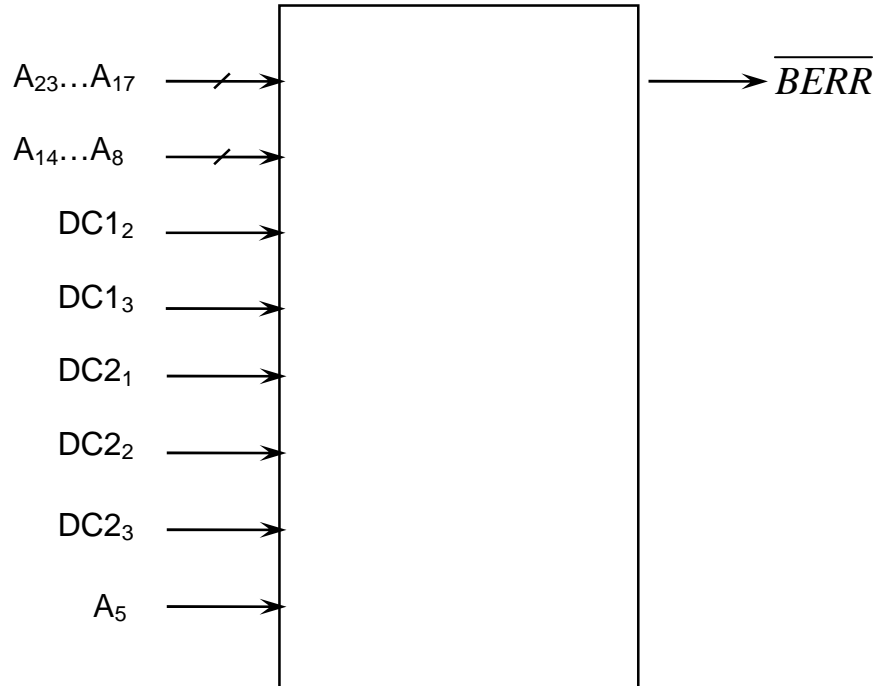
DC1, DC2.

\overline{BERR}

N5
DC1 DC2
N3

5 -

/ .



5.8 -

N5, N3, A5, A3 = A14 + ... + A8 = 0, A5 = A23 + ... + A17 = 0

- A5 = 1, $\overline{BERR} = 0$;
- DC13 = 0, $\overline{BERR} = 0$;
- DC12 = 0, A3 = 1, $\overline{BERR} = 0$;
- DC23 = 0, $\overline{BERR} = 0$;
- DC21 ^ DC22 = 0, A5 = 1, $\overline{BERR} = 0$.

()

6 ()

()

68000.

7 / (68230)

68230 [3]
(PGCR),
B(PBDDR),

(PADDR)
B(PBCR).

A(PACR)

PADR ()

PBDR ().

$A_5 \dots A_1$ (.7.1) $A_0 = 1$.

PACDR PBCDR,

7.1 – $A_5 \dots A_1$

68230

$A_5 \dots A_1$ (RS5...RS1)		
0 0 0 0	PGCR	
0 0 0 1 0	PADDR	
0 0 0 1 1	PBDDR	
0 0 1 1 0	PACR	
0 0 1 1 1	PBCR	
0 1 0 0 0	PADR	
0 1 0 0 1	P DR	

0. (00);
 (01);
 (1).

1. 16-
 (0);
 (1).
 3 4 (1
 (1 -
).
 2.

3 4-
 3. 2-
 / 16- ().

PADDR PBDDR,
 PGCR
 . 7.2, PACR PBCR - . 7.3.
 (.).

7.2 - PGCR (00000)

	7		$\frac{0}{0}(0)$	$\frac{0}{1}(1)$	$\frac{1}{0}(2)$	$\frac{1}{1}(3)$
	6					
	5	(1) 3, 4	1(0;1)	1	1	1
	4	(1) 2, 1	1(0;1)	1	1	1
	3	4	1(0)	1(0)	1(0)	1(0)
	2	3	1(0)	1(0)	1(0)	1(0)
	1	2	1(0)	1(0)	1(0)	1(0)
	0	1	1(0)	1(0)	1(0)	1(0)
1(0) -	1,	0. (0;1) - 0	1 .			

7.3 – PACR P CR

		PACR						PBCR									
		0			1			0			1			2		3	
7		0	0	1	(0)	(0)	(0)	(0)	0	0	1	(0)	(0)	(0)	(0)	(0)	(0)
6		0	1		0(0)	1(0)	(0)	(0)	0	1		0(0)	1(0)	(0)	(0)	(0)	(0)
5	2(4)*	1	1	0	0	1			1	1	0	1	1				
4		1	1			1			1	1		1	1				
3		0	0			0	0	0	0	0		0	0	0	0	0	0
2	2(4)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1(3)**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0			1				0	0		1							
* 2 – PACR 4 – P CR																	
** 1 – PACR 3 – P CR																	
–																	
		7 6 ,															

7.1

I/T

I/T , 0 1 I/T / . 32 -

[2]. 16- -

3 . 7.2 00000000 PGCR

00000000 00110000 (. 7.3). PACR PBCR -

PADDR PBDDR 00000000, -11111111. -

N5N4N3N2N1A0. A0 = 1

(/); N1 -

5... 1, . 7.1; N2 7 6 (

) / - 00; N3 - 14... 8,

0; N4
 - 10; N5
 - 0.
 8-
 PBDR
 PBDR.
 . 7.4.
 7.4 -

16 15 ()
 23... 17,
 PADR
 16-
 (A₀ = 0) -
 / -
 /

PGCR	000000010000000000(00000)1	10001
PACR	000000010000000000(00110)1	1000D
PBCR	000000010000000000(00111)1	1000F
PADDR	000000010000000000(00010)1	10005
PBDDR	000000010000000000(00011)1	10006
P DR	000000010000000000(01001)0	10012
B - , H -		
	5... 1	

PGCR
 :
 MOVEQ #0, D₁ ; D₁ 0
 MOVEA.L #10001, A₁ ; 1 10001
 MOVE.B D₁, (A₁) ;
 ; PGCR
 / .
 16- 8-
 MOVEP D_n, (0, A_n) ; D_n
 ; , / .
 ; n - P DR.
 MOVEP (0, A_n), D_n,
 8-
 MOVE.

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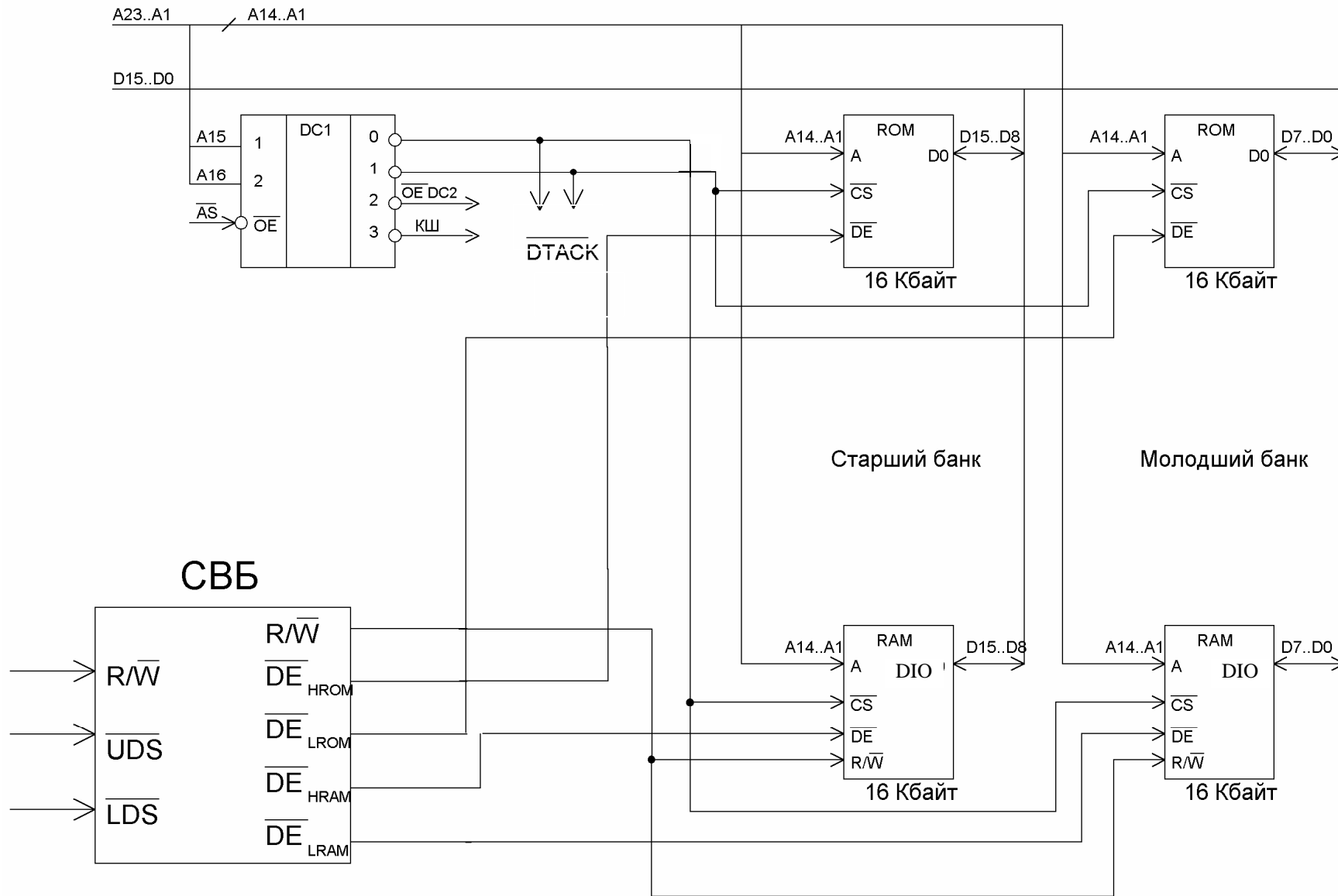
« . / . . , . . , . . . - .: » , 1988.

2

Motorola – .: . . , 1998.

3 **MC68230**. Parallel Interface / Timer (PI/T) /Advance Information, Motorola INC, 1983.

4 **MC68681**. Dual Asynchronous Receiver / Transmitter (DUART) / Advance Information, Motorola INC, 1985.



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