Ministry of Transport and Communications of Ukraine

.....

State Administration of Communications of Ukraine

.....

Odessa National Academy of Telecommunications after A.S. Popov

Department of Computer Science and Microprocessors

Computer Science and Microprocessors

Module №2

Programming of Intel microprocessors

for students

SERIAL PORT RS-232-C

training area: telecommunications

for specialties: 7. 092402, 7. 092401, 7. 092404, 7. 092407

Odessa 2009

УДК План НМВ 2009 р.

Writer: Tkachenko A.A.

In the methodical guide there are the structure and the programming's modes of serial port RS-232-C. The variants of home tasks and order of the laboratory work execution are presented.

IT IS APPROVED
by methodical council
of academy
Minutes № 6
from 10.02.2009

IT IS APPROVED
on department meeting
of Computer Science
and Microprocessors and
recommended for
printing
Minutes № 3
from 10.10.2008

I. Foreword

Discipline general characteristic (quantity of credits ECTS - 6; modules - 4; substantial modules - 14; total hours - 216; including: lectures - 68 h.; laboratory works - 32 h.; practical trainings - 0 h.; independent work - 58 h.; individual work - 58 h.; semester 2.3, 2.4, 3.1, 3.2, a control kind: the complex task, the course work, the test.

II. The purpose of discipline training

The purpose and subject matter of problems: knowledge formation concerning computer aids construction principles and microprocessor systems, creation and software debugging of them, ability to analyse, working out and operate such systems in telecommunications.

III. The discipline content

Electronic computers nodes of: digital automatic machines, both their analysis and synthesis; memory devices, their classification and the organization; microprocessors (MP), construction principles and microprocessors and electronic computers functioning, universal microprocessors architecture, the organisation of memory and ways of addressing of operands in microprocessors.

Microprocessor systems (MPS): construction principles, ways of the organisation of data exchange in MPS, address space and its distribution in MPS, typical user MPS interface hardware and program means, the interruptions organisation in MPS; controllers in telecommunications, microcontrollers of conducting firms, control means and switching construction in systems of telecommunications at hardware and program levels; digital signals processors in telecommunications, conducting firms digital signals processors, telecommunications systems signals transformation modules construction on hardware and program levels; MPS productivity increase , multiprocessing system.

The MPS software: programming of MT INTEL firm, the raised word length MT programming of conducting firms; microcontrollers and processors digital signals programming.

The module 1: Units of computer facilities and microprocessor systems

Entrance requirements to module studying (knowledge and abilities from disciplines which provide studying of the given module).

№	Content of knowledge	Code number
1	Number representations	KN.1
2	Circuitry bases	KN.2
	Content of abilities	
1	Designing of communication networks	AB.1
2	Communication networks tumimg	AB.2

Structure of the test module 1

The substantial module	Lecture (hours)	Study		Self-instruction	Individual work
		practical	laboratory		
The module 1: The nodes of computer facilities and microprocessor systems (2 credits; 52 h.)					
1. Computer aids	4		2	2	2
2. Microprocessors	6		2	4	4
3. Memory subsystems	4		2	4	4
4. Interfaces	2		2	4	4
1 module in total, h.	16	–	8	14	14

Content of substantial modules (lecture hours - 16):

1.1 Computer aids (4 h.)
The content: Computer and microprocessor systems.; Data manipulation in computer systems.

1.2 Microprocessors (6 h.)
The content: Digital automaton. Digital automata synthesis.; Typical computer systems devices.; Microprocessors architecture. Software models of the 16- and 32-bit Intel microprocessors.

1.3 Memory subsystems (4 h.)
The content: Memory construction principles with the set organization.; Address space and its distribution in MPS. Memory segmentation. Operand addressing modes for the Intel microprocessors.

1.4 Interfaces (2 h.)
The content: Principles of the computer construction and its functioning. Interfaces.

Laboratory studies' themes of the module 1

№	NUMBER, THE NAME OF LABORATORY WORKS	Hours
1	Arithmetic logic unit	2
2	Storage device	2
3	Architecture and software models of Intel microprocessors	2
4	Memory segmentation	2
	In total	8

Initial knowledge and abilities from the module 1

№	Content of knowledge	The code number
1	To know the construction principles of arithmetic logic and memory devices	KN.1
2	To know architecture and operand addressing modes for the Intel microprocessors.	KN.2
	Content of abilities	
1	To submit and treat entrance and initial numerical data for the further digital processing. To correlate logic changes and functions to digital signals which realize them.	AB.1
2	To put and solve the problems connected with the analysis, working out and operation of microprocessor systems of different function, creation and to software debugging to them.	AB.2

The module 2: Programming of Intel microprocessors.

Entrance requirements to module studying (knowledge and abilities from disciplines which provide studying of the given module).

№	Content of knowledge	The code number
1	Number representations	KN.1
2	Circuitry bases	KN.2
3	The general principles of programming	KN.3
	Content of abilities	
1	Designing of communication networks	AB.1
2	Communication networks tumimg	AB.2

Structure of the test module 2

The substantial module	Lecture (hours)	Employment		Self-instruction	Individual work
		practical	laboratory		
The module 2: Intel microprocessors programming (1 credit; 56 h.)					
1.Programming language Assembler-86	2		2	5	5
2.The linear program organizations using Assembler-86	2		2	5	5
3.The branched and cyclic programs organization using Assembler-86 language	14		4	5	5
1 module in total, h.	18	–	8	15	15

Content of substantial modules (lecture hours - 18):

2.1 Programming language Assembler-86 (2 h.)
The content: Low-level programming languages. Assembly programming language. Instruction and data formats. Operand addressing modes. Move instructions.

2.2 The linear program organisation using Assembly language (2 h.)
The content: Data conversion instruction in Assembly language. The linear programs.

2.3 The branched and cyclic programs organisation using Assembly language
The content: Conditional and unconditional jump instructions in Assembly language. The branched programs.; The organisation of cyclic programs.; Data exchange modes in MPS. The user interface software in typical MPS.; Organization of interrupts in MPS. Types of interrupts.; Productivity of microprocessors and estimation of it. Architecture of modern microprocessors.; Intel microprocessors using in telecommunication. Software support of telecommunications facilities nodes.

Laboratory studies' themes of the module 2

№	NUMBER, THE NAME OF LABORATORY WORKS	Hours
1	The linear programs	2
2	The branched programs	2
3	The cyclic programs	2
4	Serial port RS-232-C	2
	In total	8

Initial knowledge and abilities from the module 2

№	Content of knowledge	The code number
1	To know the operand addressing modes, move instructions, conditional and unconditional jump instructions, organisation interrupts in MPS .	KN.1
2	To know the software support of telecommunications facilities nodes.	KN.2
	Content of abilities	
1	To put and solve the problems connected with the analysis, working out and operation of different functional MPS, creation and software debugging of them.	AB.1
2	To analyze and develop separate telecommunications systems nodes which use computer means and microprocessors. To use typical digital blocks, nodes and elements for digital devices realization.	AB.2
3	To put and solve the problems connected with a computer means choice, microprocessors behind their technical, operational and economic characteristics for systems of telecommunications.	AB.3

The module 3: Microprocessor systems (MPS) on universal microprocessors and its programming

Entrance requirements to module studying (knowledge and ability from disciplines which provide studying of the given module).

№	Content of knowledge	The code number
1	The general MPS architecture	KN.1
2	Microprocessors programming bases	KN.2
	Content of abilities	
1	Communication networks designing	AB.1
2	Communication networks tumimg	AB.2

Structure of the test module 3

The substantial module	Lecture (hours)	Employment		Self-instruction	Individual work
		practical	laboratory		
The module 3: Microprocessor systems (MPS) on universal microprocessors and its programming (2 credits; 52 ч.)					
1. x-bit Motorola microprocessors	4		2	4	4
2. MPS construction on 32-bit Motorola MP	6		2	5	5
3. MPS software creation on 32-bit Motorola MP	6		4	5	5
1 module in total, h.	16	–	8	14	14

Content of substantial modules (lecture hours - 16):

3.1 x-bit Motorola microprocessors (4 h.)
The content: Motorola MP MC68XXX. Software models of MP MC68000 and 68020.; Memory organisation and operand addressing modes in MP MC68XXX .

3.2 MPS construction on 32-bit Motorola MP (6 h.)
The content: Principles of MPS construction on MP MC68XXX.; Distribution of address space in MPS on MP MC68XXX. The organisation of a memory subsystem.; The organisation of a peripheral subsystem.

3.3 Creation of the software for MPS on 32-bit Motorola MP (6 ч.)
The content: Instruction set of MP MC68000. Examples of programs with different operand addressing modes in instructions.; Control transfer instruction in MP MC68XXX.; Construction of programs with structure "branching" and "cycle" in MP MC68XXX.

Laboratory studies' themes of the module 3

№	NUMBER, THE NAME OF LABORATORY WORKS	Hours
1	Monitor instructions studying of Motorola MC 68xxx	2
2	Structure and operand addressing modes of typical instructions in Motorola MP 68xxx	2
3	Instruction set of Motorola MP 68xxx	2
4	Programming of Motorola MP 68xxx	2
	In total	8

Initial knowledge and abilities from the module 3

№	Content of knowledge	The code number
1	To know the structure and addressing modes in typical commands of Motorola MP 68xxx.	KN.1
2	MPS construction principles. Memory subsystem organisation. Peripheral subsystem organisation.	KN.2
	Content of abilities	
1	To put and solve the problems connected with the analysis, working out and microprocessor systems operation of different function, creation of the software debugging them.	AB.1
2	To analyze and develop separate telecommunications systems nodes which use computer aids, microprocessors and microcontrollers. To use typical digital blocks, nodes and elements for digital devices realization.	AB.2

The module 4: Microprocessor systems on microcontrollers and DSP and its programming.

Entrance requirements to module studying (knowledge and ability from disciplines which provide studying of the given module).

№	Content of knowledge	The code number
1	General MPS architecture	KN.1
2	Microprocessors programming bases	KN.2
	Content of abilities	
1	Communication networks designing	AB.1
2	Communication networks tumimg	AB.2

Structure of the test module 4

The substantial module	Lecture (hours)	Employment		Self-instruction	Individual work
		practical	laboratory		
The module 4: Microprocessor systems on microcontrollers and DSP and its programming (1 credit; 56 h.)					
1. Motorola microcontrollers	4		2	2	2
2. MPS construction on Motorola MC	4		2	3	3
3. Software creation for MPS on Motorola MC	6		2	5	5
4. Digital signals processors	4		2	5	5
1 module in total, h.	18	–	8	15	15

Content of substantial modules (lecture hours - 16):

4.1 Motorola microcontrollers (4 h.)
The content: Motorola Microcontrollers (MC): HC05, HC08, HC11. Structure; MC intrinsics.

4.2 MPS construction on Motorola MC (4 h.)
The content: Adjustment of the MC intrinsics.; Typical MC programming examples.

4.3 Software creation for MPS on Motorola MC (6 h.)
The content: Motorola RISC-processors; General principles of the digital signals processing.; Construction principles of telecommunications nodes at program level.

4.4 Digital signals processors (4 h.)
The content: Architecture and construction principles of digital processors (DSP), its features and field of use.; Microprocessor systems in terms of the DSP, universal MP and MC.

Laboratory studies' themes of the module 4

№	NUMBER, THE NAME OF LABORATORY WORKS	Hours
1	The organisation branched programs in Motorola MP 68xxx using Assembly language	2
2	The organisation cyclic programs in Motorola MP 68xxx using Assembly language	2
3	Instruction set of Motorola 68HC05microcontroller	2
4	Motorola 68HC05 microcontroller processor module and technological features structure studying.	2
	In total	8

Initial knowledge and abilities from the module 4

№	Content of knowledge	The code number
1	To know Instruction set of the Motorola 68HC05 microcontroller, processor module structure and technological features of the microcontroller.	KN.1
	Content of abilities	
1	To put and solve the problems connected with a computer aids choice, microprocessors and microcontrollers behind its technical, operational and economic characteristics for telecommunications systems.	AB.1
2	To create and adjust the software for digital signals processing devices in telecommunications systems using languages of specific microprocessors and microcontrollers.	AB.2
3	To submit and treat entrance and initial numerical data for the further digital processing. To correlate logic changes and functions to digital signals which realize its.	AB.3

1. Study objective

An acquaintance with possibilities and scope of serial port's RS-232-C use, modes of its programming.

2. Key points

Serial port RS-232-C, that is named an asynchronous adapter or serial interface is used for many purposes:

– connection of mouse;

– connection of scanners, printers, digitizers;

– implementation of connection between two computers with using of special cable and shell Norton Commander;

– connection of modems for data transmission by telephone lines;

– connection to the personal computer network.

Every computer has at least one serial port for data exchange.

2.1. Communications protocol

Communications protocol consists of transmission description and purposes of its components.

Serial data transmission means that information is passed by one transmission line. On figure 2.1 there are the form of electric signals and data format when the ASCII character A (41H) is transferred:

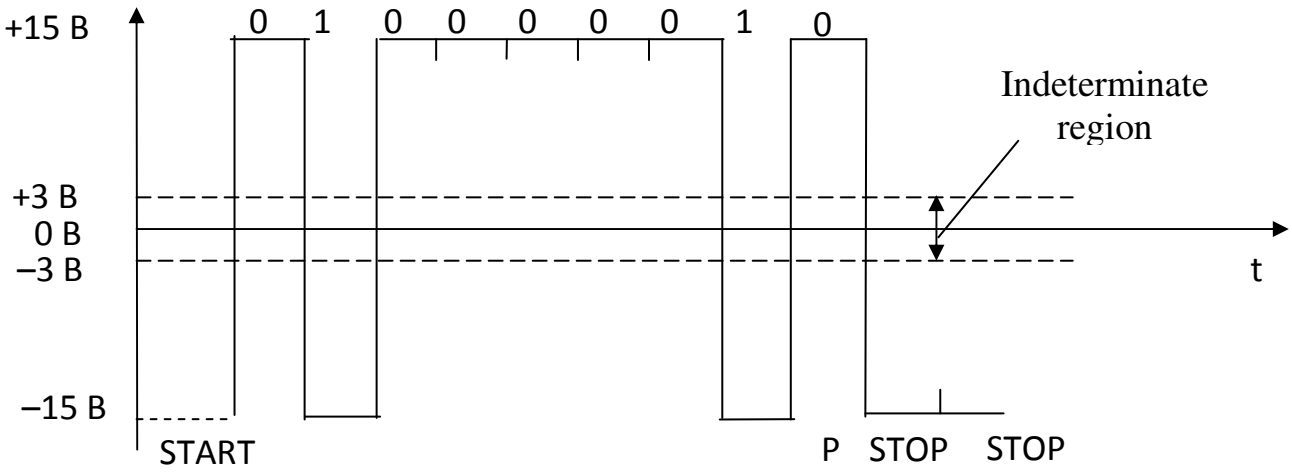


Figure 2.1 – The timing chart of electric signals and data format for datum 41H

A zero level equals +15 V and one level is –15 V. Initial state of line is "1". Start bit signals about beginning of data transmission; the bits of information are passed in such order: D0–D1–D2–D3–D4–D5.... If the parity bit P is used, it is transmitted also. The parity bit has to have such value, that the package of bits contains even or odd number of binary ones (or zeros). At the end one or two stop

bits are transmitted and complete transmission. Then the level of line again is set in one level that equals to -15V. The use of parity, start and stop bits is determined by communications protocol.

Other important feature is data transfer rate. It must be identical for a transmitter and receiver. Data transfer rate is measured in bauds (a baud is an amount of bits which are passed per second). Start-stop bits and parity bit are also taken into account. Other term is sometimes used as bits per second (bps). It means effective data transfer rate discarding the service bits.

2.2. Hardware implementation

A computer has from one to eight serial ports, which are realized on the microcircuit Intel 8250. It is an universal asynchronous receiver-transmitter (UART). A microcircuit contains a few internal registers, accessible to the input/output instructions. During transmission the byte is written into the buffer register of transmitter and then it is transcribed into the shift register of transmitter. A byte is „pulled out" from a register by bits, low bits forward. Analogously a receiver also has shift and buffer registers. Peripheral devices connect to input/output port through a connector DB25P or DB9P, which has 25 and 9 pins respectively. On figure 2.2 there is given graphic image of microcircuit of Intel 8250. Below is a table 2.1 of pin connections for the 9 pin D-Type connectors.

Table 2.1 – Purposes of connector pins

Pin number	Purpose of pin	Input or output
1	Data and Carrier Detect (DCD)	Input
2	Receive Data (RD)	Input
3	Transmit Data (TD)	Output
4	Data Terminal Ready (DTR)	Output
5	Signal Ground (SG)	Output
6	Data Set Ready (DSR)	Input
7	Request To Send (RTS)	Output
8	Clear To Send (CTS)	Input
9	Ring Indicator (RI)	Input

2.3. Ports of asynchronous adapter

During computer initialising the module POST BIOS tests legacy asynchronous adapters and initialise the first two of them. Their base addresses are located in the BIOS data area beginning from the address 0000:0400H. The first adapter, COM1, has a base address 3F8H and occupies the address range from 3F8H to 3FFH. The second adapter, COM2, has a base address of 2F8H and occupies the addresses from 2F8H to 2FFH. Asynchronous adapters can cause interrupts: COM1 – IRQ4 (INT 0CH), COM2 – IRQ3 (INT 0BH).

2.3.1. Port 3F8H

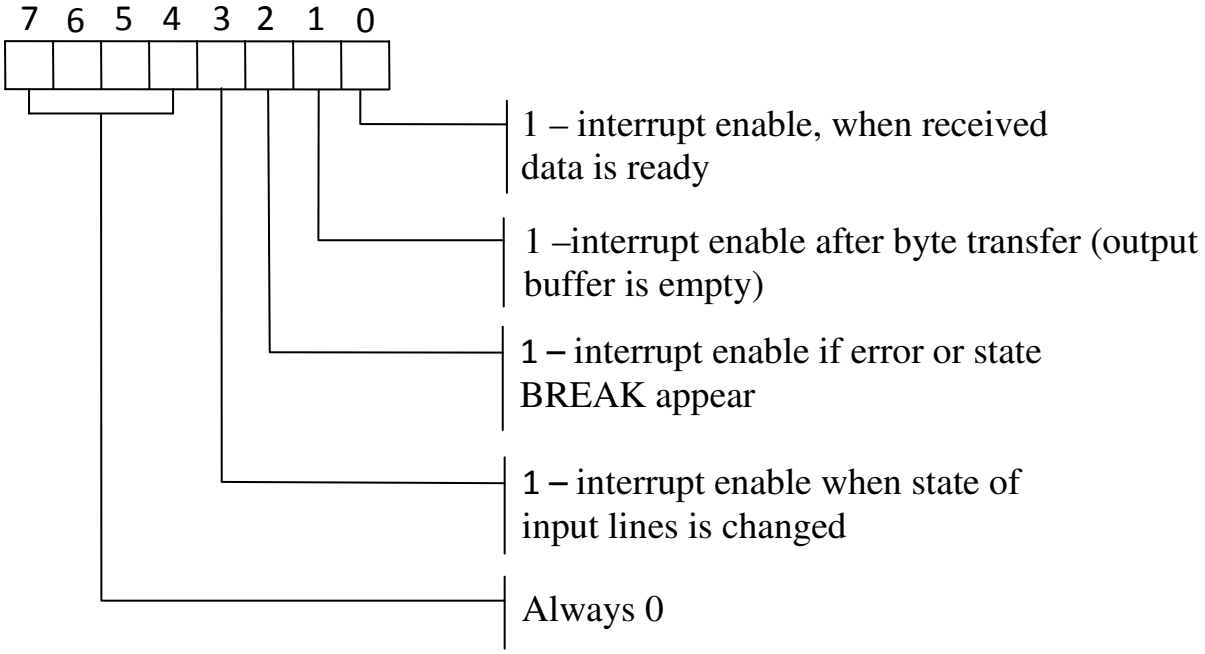
The port 3F8H fit with the data register. For data transfer they need to be written into this port. After receipt of data from a peripheral device they can be read from this port.

The purpose of port 3F8H can change, depending on the state of high-order bit of control word which inputs into a control register with the address 3FBH. If this bit is 0, port 3F8H is utilized for the record of transferable data. If it is equal to 1, 3F8H port is utilized for the output of low byte of frequency divider in time generator. Changing the value of frequency divider, we can change rate of port working. The high byte of divider is written into port 3F9H. Dependence of data transfer rate on the value of frequency divider is stated below:

Divider	Rate (Baud)
1040	110
768	150
384	300
192	600
96	1200
48	2400
24	4800
12	9600
6	19200
3	38400
2	57600
1	115200

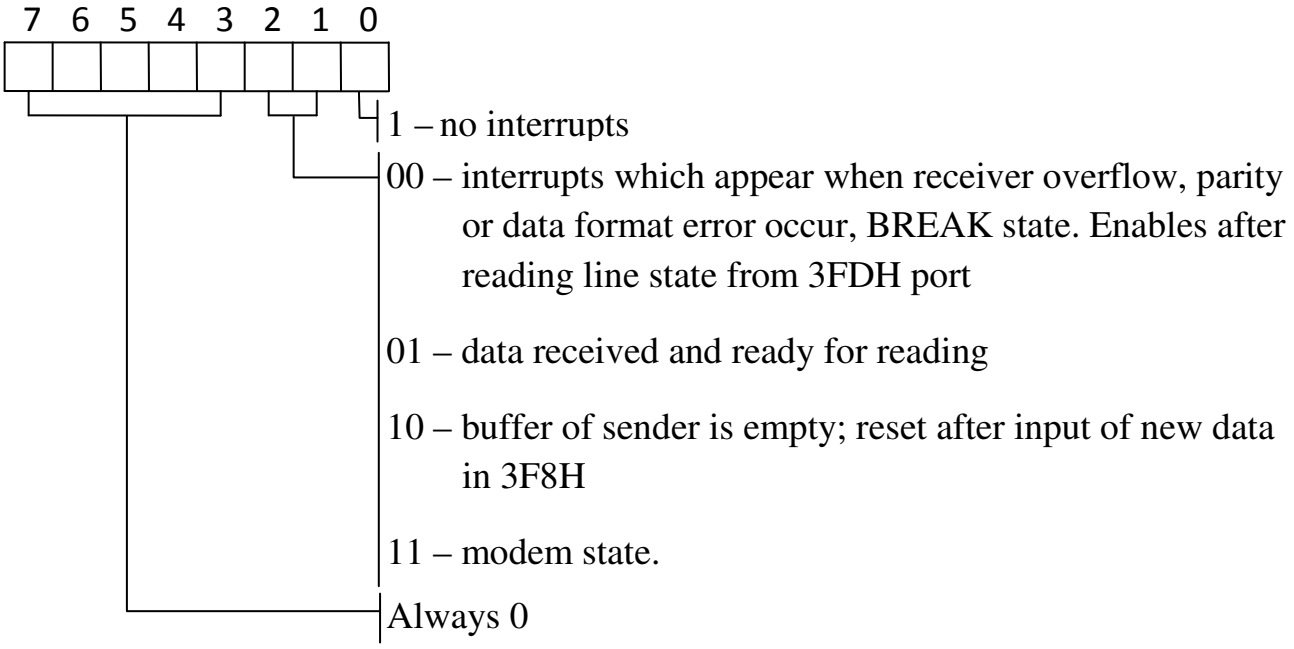
2.3.2. Port 3F9H

Port is utilized as an interrupt control register of the asynchronous adapter or (after an output into port 3F8H byte with set unit in high-order bit) for the output of high byte of frequency divider. In the mode of interrupt control port has such format:



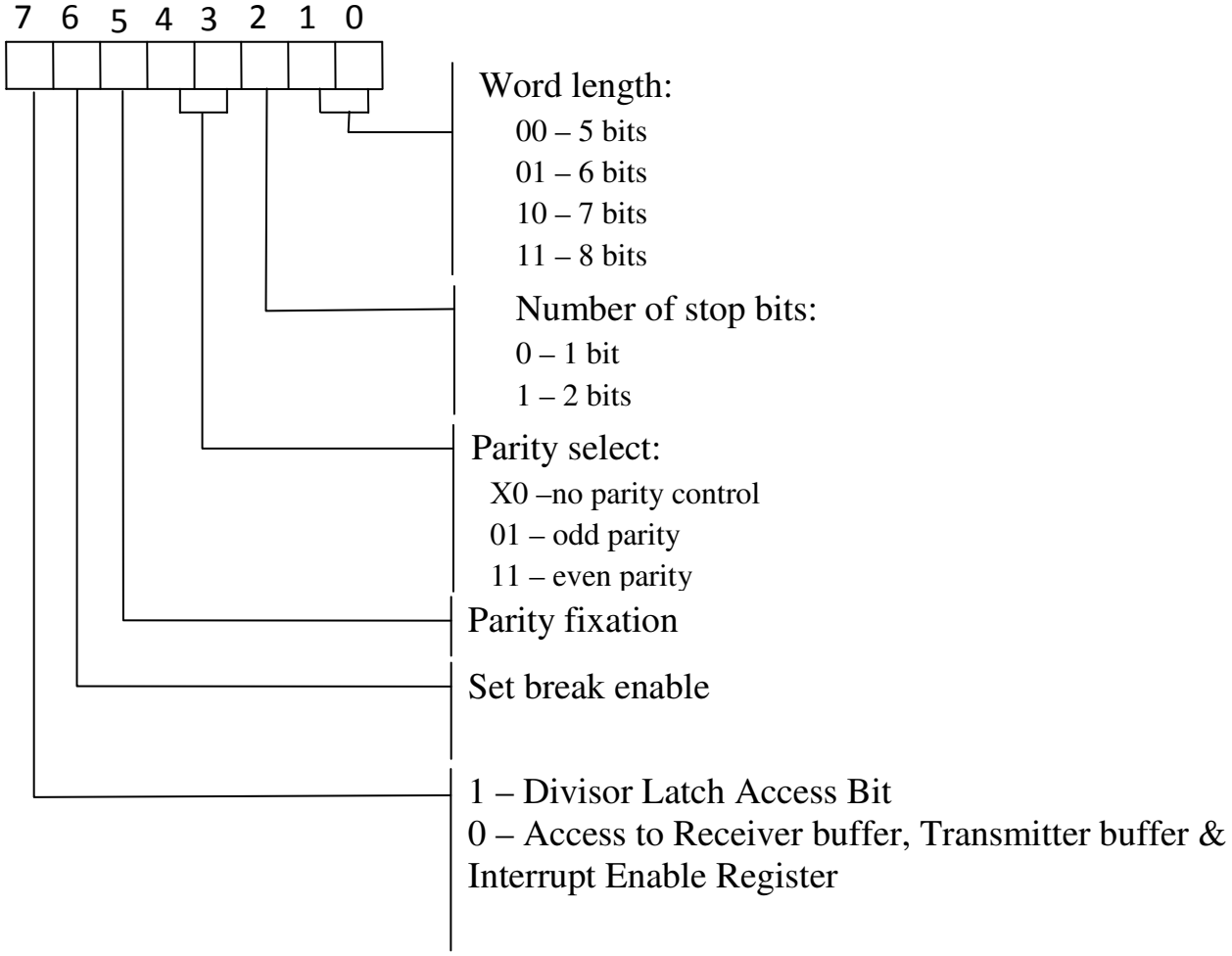
2.3.3. Port 3FAH

A register is intended for authentication of interrupts. Its content determines reason of interrupt. A register has such format:



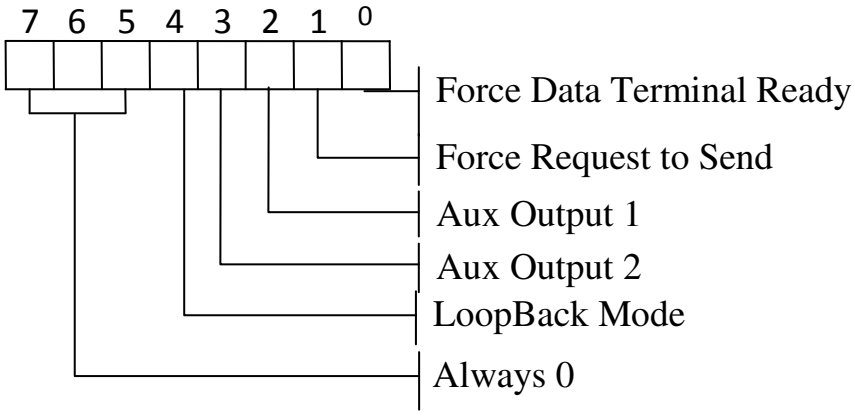
2.3.4. Port 3FBH

Line control register, accessible for a record and read-out.



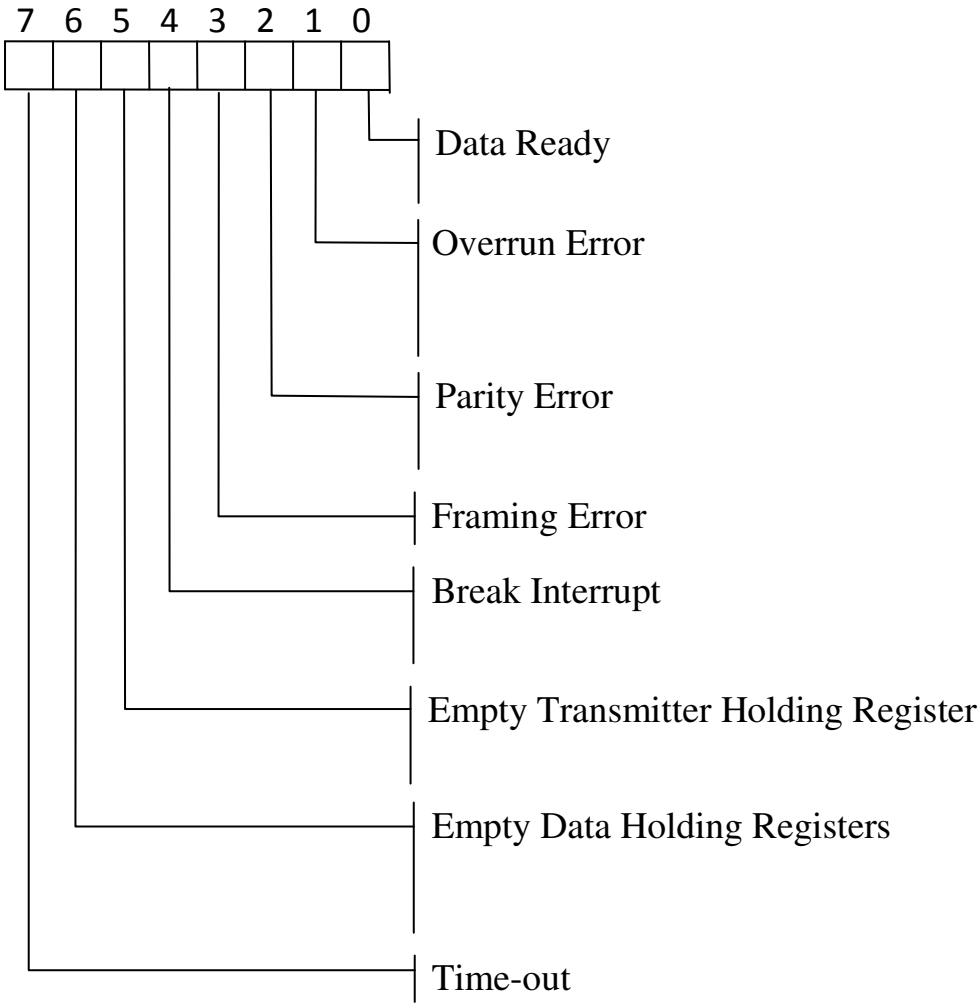
2.3.5. Port 3FCH

The modem control register is a read/write register. Bits 5,6 and 7 are reserved. Bit 4 activates the loopback mode. In Loopback mode the transmitter serial output is placed into marking state. The receiver serial input is disconnected. The transmitter out is looped back to the receiver in. DSR, CTS, RI & DCD are disconnected. DTR, RTS, OUT1 & OUT2 are connected to the modem control inputs. The modem control output pins are then place in an inactive state. In this mode any data which is placed in the transmitter registers for output is received by the receiver circuitry on the same chip and is available at the receiver buffer. This can be used to test the UARTs operation. Format of port:



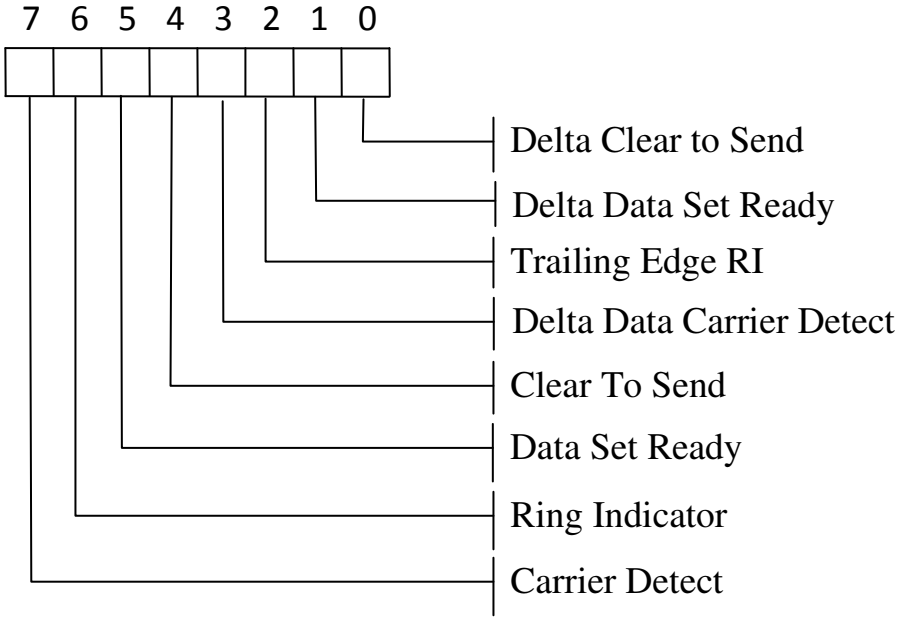
2.3.6. Port 3FDH

The line status register is a read only register.



2.3.7. Port 3FEH

Modem status register.



2.4. Programming of asynchronous adapter

2.4.1. Initialising of asynchronous adapter

At first, the program which works with an asynchronous adapter must set communications protocol and data transfer rate. After the load of the operating system the speed is set 2400 Baud, an parity check is not executed, one stop bit and 8-bit length of transferable character is utilized.

At entry the program can get the current mode of adapter from port 3FBH, for example, it is possible to read a adapter status byte 000X0011=03H (or 13H) from control register 3FBH after load of BIOS. For setting of other mode it is possible to change the necessary fields and write down the new byte of the mode to address 3FBH. For example, the control word 00011110B=1EH corresponds to the mode of port, represented on figure 2.1.

For setting of new value of data transfer rate it is necessary to set the high-order bit of control byte as 1 and output 80H to address 3FBH. After that it is necessary to load the frequency divider. The low byte of divider is loaded into port 3FBH, and high byte – into port 3F9H. Before the beginning of work the interrupt control register (port 3F9H) must be initialized, even if interrupts from adapter are not utilized. If interrupt is not needed, a zero is written down into the port. Initialising is complete.

Before a record the data byte it is necessary to check the storage register of transmitter. It must be free. The sign of „empty” storage register is set 1 in fifth bit of line status register to the address 3FDH.

At data accepting before input of character from receiver port 3F8H it is necessary to check up the value of 0 bit of the port 3FDH. If it is equal 1, character is accepted from a line and the last is in the buffer register of receiver.

For permission of interrupts it is necessary to set the corresponding bits of interrupt control port 3F9H in "1". When interrupt takes place, the interrupt handler must analyse its reason by value of interrupt identification port's content with the address 3FAH. At the end of the program-handler of hardware interrupt there must be instructions sequence:

```
MOV AL,20H
OUT 20H,AL
IRET
```

If at the same time there are a few interrupt requests, a 0 bit of authentication register will be set in 1. In this case before completion of interrupt processing it is necessary to read again the interrupt authentication register and handle the next interrupt. A process repeats until a 0 bit of interrupt authentication register will not be equal to 0.

2.4.2. Sample of data's input/output initialization routine with use of language Assembler-86

```
        MOV DX,3FBH   ; load of control register's address into DX

        IN    AL,DX   ; input of the adapter's current mode
                      ; after the load of BIOS: speed is 2400 Baud; (divisor is
                      ; 30H), there is not parity control (D3=0 ; D4=X), one stop
                      ; bit (D2=0), amount of bits is 8 (D1=1, D0=1), a status
                      ; word is equal 000X0011=03H or 13H
        MOV AL,80H    ; control port adapts for transfer of divisor: D7=1,
                      ; other bits are equal to 0, a control word is equal 80H
        OUT DX,AL     ; output of the control word
        MOV DX,3F8H   ; load of port's 3F8H address
                      ; and
        MOV AL,60H    ; load of low byte
        OUT DX,AL     ; of frequency divider

        MOV DX,3F9H   ; load of port's 3F9H address
                      ; and
        MOV AL,00H    ; load of high byte
        OUT DX,AL     ; of  frequency divider
                      ;
M3:     MOV AL,1E     ; load of control word into AL
        MOV DX,3FBH   ; load of control register's address
        OUT DX,AL     ; output of the control word
        MOV AL,00H    ; interrupt disable from RS-232-C
```

```
        MOV DX,3F9H    ; load of interrupt control register's address
        OUT  DX,AL     ; output of the control word

M1:     MOV DX,3FDH    ; load of  line status register's address
        IN     AL,DX   ; input of the control word

        AND  AL,20H    ; storage register
        JZ     M1      ; is empty, D5=1?

        MOV AL,41H     ; yes, load datum into AL
        MOV DX,3F8H    ; load of  data transfer port's address
        OUT  DX,AL     ; output of data

        MOV DX,3FDH    ; load of  line status register's address

M2:     IN     AL,DX   ; input of status line word

        AND AL,01H     ; verification of data presence in a line (D0=1?)
        JZ     M2      ; in the loop

        MOV DX,3F8H    ; load of  data transfer port's address
M5:     IN     AL,DX   ; input of data
        JMP  M4        ; cycling of the program
        NOP
```

It is necessary to state the effective addresses instead of marks at implementation of the program in debug monitor.

The program allows in the step-by-step mode to carry out the input of the status word of adapter's mode after the load of the operating system, initialize an adapter, to check up consisting of transmit-data buffer at data transfer and presence of data in line at accepting.

2.4.3. Sample of data's input/output initialization routine with use of language TURBO ASSEMBLER (TASM)

```
; Initialization routine of serial adapter and data input/output TITLE
  RS232.ASM

MODEL SMALL
STACK 256
DATA SEGMENT
DATA ENDS
CODE SEGMENT
ASSUME CS:CODE, DS:DATA, ES:DATA
```

```
START:  MOV     AX,DATA  ; data
        MOV     DS,AX    ; segments'
        MOV     ES,AX    ; combination
        MOV     DX,3FBH  ; setting
        MOV     AL,80H   ;
        OUT     DX,AL    ; of
        MOV     DX,3F8H  ;
        MOV     AL,60H   ;
        OUT     DX,AL    ; generator's
        MOV     DX,3F9H  ;
        MOV     AL,00H   ; frequency divider
        OUT     DX,AL    ;

    ; Setting of the adapter's new mode
CONTR:  MOV     AL,1E    ; load
        MOV     DX,3FBH  ; the control
        OUT     DX,AL    ; word (1AH)

INTER:  MOV     AL,00H   ; interrupt
        MOV     DX,3F9H  ; disable
        OUT     DX,AL    ; from RS-232-C
    ; Data transfer
STATUS: MOV     DX,3FDH  ; verification
        IN      AL,DX    ; to the state
        AND     AL,20H   ; buffer of port
        JZ      STATUS   ; in the loop

SEND:   MOV     AL,41H   ; transfer
        MOV     DX,3F8H  ; of datum
        OUT     DX,AL    ; 52H

    ; Accepting of data
        MOV     DX,3FDH  ; test
READY:  IN      AL,DX    ; for the presence
        AND     AL,01H   ; of data
        JZ      READY    ; in a line
        MOV     DX,3F8H  ; at data
        IN      AL,DX    ; accepting
        JMP     STATUS   ; cycling of the program
        NOP
EXIT:   MOV     AH,4CH   ; program
        INT     21H      ; exit
    CODE ENDS
    END
```

3. Control questions

3.1 What functions are executed by an asynchronous serial adapter?

3.2 What devices which are part of computer, connects by the adapter RS-232-C?

3.3 What priority do computer ports COM1 and COM2 have?

3.4 What mode of adapter working is set at the loading of the operating system?

3.5 How is data transfer rate set in the adapter?

3.6 What ports are contained by the adapter?

3.7 What is the communications protocol?

3.8 What information is contained by a control word which sets the mode of adapter working?

3.9 For what purpose are word of line's status at accepting and the word of buffer's status at the transfer read out?

4. Homework

4.1 Set the necessary amount of bits for transfer by an asynchronous serial adapter of datum, which corresponds to two last numbers of student's card.

4.2 Set one (even variant) or two (odd variant) stop bits and odd or even parity depending on the variant of task. Evenness or oddness of variant is defined by next to last figure of student's card.

4.3 Make a control word according to the set adapter's behaviour.

4.4 Make initialization routine of adapter, transfer and accepting of datum with comments to instructions.

4.5 Give the timing chart of electric signals and datum format according to your variant.

4.6 Give the answers to control questions.

5. Laboratory task

5.1 Invoke the initialization routine of adapter from memory of computer in debug monitor by directive

L 7000:100

5.2 Input into the program the setting of initialising and your datum.

5.3 Execute the program in step-by-step mode.

5.4 Make sure that transmitted information is accepted by the adapter.

5.5 Invoke the program from memory of computer using of TASM from the library of ASM:RS232.ASM.

5.6 Input into the program the setting of the mode and your data.

5.7 Generate the object module RS232.obj and printout by the compiler of TASM.EXE.

5.8 Make sure that program errors are absent.

5.9 Generate the executable module RS232.EXE by the program TLINK.EXE.

5.10 Start the program RS232.EXE (it will be executed in the infinite loop).

5.11 Look after the timing chart of data transfer/accepting on the contacts 2–3 of port COM1.

5.12 Analyse timing charts, select on them start, informative, stop bits, parity bit. Compare the resulted timing charts with draw up in homework.

6. Contents of the protocol

Protocol must have the title of laboratory work and its purpose, results of the homework processing according to the requirements of item 4, notes to results of programs implementation in the step-by-step mode, timing chart from the screen of oscillograph, conclusions to implementation of laboratory work.

7. The literature list

8.1 Майко Г.В. Ассемблер для IBM PC. – М.: Бизнес-информ, Сирин, 1997.

8.2 Фролов А.В., Фролов Г.В. Аппаратное обеспечение IBM PC. – Т.2, ч. 1. – М.: Диалог-МИФИ, 1992.

8.3 RS232 C/D/E Connection Information. – http://users.breathemail.net/trevor_gowen/rs232.htm, 20.05.2000.

8.4 http://www.beyondlogic.org/serial/serial.htm#1, 15.01.2009.