Ministry of Transport and Communications of Ukraine

State Administration of Communications of Ukraine

Odessa National Academy of Telecommunications after A.S. Popov

Department of Computer Science and Microprocessors

Computer Science and Microprocessors

Module №1

Units of computer facilities and microprocessor systems

for students

STORAGE DEVICE

training area: telecommunications

for specialties: 7. 092402, 7. 092401, 7. 092404, 7. 092407

Odessa 2009

УДК План НМВ 2009 р.

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The organisation of the storage devices is considered. Research of a read-only and random-access memories (ROM and RAM) is carried out in the laboratory work. The scheme and the description of laboratory installation, variants of tasks and order of the laboratory work execution are presented.

IT IS APPROVED
by methodical council
of academy
Minutes № 6
from 10.02.2009

IT IS APPROVED
on department meeting
of Computer Science
and Microprocessors and
recommended for
printing
Minutes № 3
from 10.10.2008

I. Foreword

Discipline general characteristic (quantity of credits ECTS - 6; modules - 4; substantial modules - 14; total hours - 216; including: lectures - 68 h.; laboratory works - 32 h.; practical trainings - 0 h.; independent work - 58 h.; individual work - 58 h.; semester 2.3, 2.4, 3.1, 3.2, a control kind: the complex task, the course work, the test.

II. The purpose of discipline training

The purpose and subject matter of problems: knowledge formation concerning computer aids construction principles and microprocessor systems, creation and software debugging of them, ability to analyse, working out and operate such systems in telecommunications.

III. The discipline content

Electronic computers nodes of: digital automatic machines, both their analysis and synthesis; memory devices, their classification and the organization; microprocessors (MP), construction principles and microprocessors and electronic computers functioning, universal microprocessors architecture, the organisation of memory and ways of addressing of operands in microprocessors.

Microprocessor systems (MPS): construction principles, ways of the organisation of data exchange in MPS, address space and its distribution in MPS, typical user MPS interface hardware and program means, the interruptions organisation in MPS; controllers in telecommunications, microcontrollers of conducting firms, control means and switching construction in systems of telecommunications at hardware and program levels; digital signals processors in telecommunications, conducting firms digital signals processors, telecommunications systems signals transformation modules construction on hardware and program levels; MPS productivity increase , multiprocessing system.

The MPS software: programming of MT INTEL firm, the raised word length MT programming of conducting firms; microcontrollers and processors digital signals programming.

The module 1: Units of computer facilities and microprocessor systems

Entrance requirements to module studying (knowledge and abilities from disciplines which provide studying of the given module).

№	The content of knowledge	The code number
1	Number representations	KN.1
2	Circuitry bases	KN.2
	The content of abilities	
1	Designing of communication networks	AB.1
2	Communication networks tumimg	AB.2

Structure of the test module 1

The substantial module	Lecture (hours)	Study		Self-instruction	Individual work
		practical	laboratory		
The module 1: The nodes of computer facilities and microprocessor systems (2 credits; 52 h.)					
1. Computer aids	4		2	2	2
2. Microprocessors	6		2	4	4
3. Memory subsystems	4		2	4	4
4. Interfaces	2		2	4	4
1 module in total, h.	16	–	8	14	14

The content of substantial modules (lecture hours - 16):

1.1 Computer aids (4 h.)
The content: Computer and microprocessor systems.; Data manipulation in computer systems.

1.2 Microprocessors (6 h.)
The content: Digital automaton. Digital automata synthesis.; Typical computer systems devices.; Microprocessors architecture. Software models of the 16- and 32-bit Intel microprocessors.

1.3 Memory subsystems (4 h.)
The content: Memory construction principles with the set organization.; Address space and its distribution in MPS. Memory segmentation. Operand addressing modes for the Intel microprocessors.

1.4 Interfaces (2 h.)
The content: Principles of the computer construction and its functioning. Interfaces.

Laboratory studies' themes of the module 1

№	NUMBER, THE NAME OF LABORATORY WORKS	Hours
1	Arithmetic logic unit	2
2	Storage device	2
3	Architecture and software models of Intel microprocessors	2
4	Memory segmentation	2
	In total	8

Initial knowledge and abilities from the module 1

№	The content of knowledge	The code number
1	To know the construction principles of arithmetic logic and memory devices	KN.1
2	To know architecture and operand addressing modes for the Intel microprocessors.	KN.2
	The content of abilities	
1	To submit and treat entrance and initial numerical data for the further digital processing. To correlate logic changes and functions to digital signals which realize them.	AB.1
2	To put and solve the problems connected with the analysis, working out and operation of microprocessor systems of different function, creation and to software debugging to them.	AB.2

The module 2: Programming of Intel microprocessors.

Entrance requirements to module studying (knowledge and abilities from disciplines which provide studying of the given module).

№	The content of knowledge	The code number
1	Number representations	KN.1
2	Circuitry bases	KN.2
3	The general principles of programming	KN.3
	The content of abilities	
1	Designing of communication networks	AB.1
2	Communication networks tumimg	AB.2

Structure of the test module 2

The substantial module	Lecture (hours)	Employment		Self-instruction	Individual work
		practical	laboratory		
The module 2: Intel microprocessors programming (1 credit; 56 h.)					
1.Programming language Assembler-86	2		2	5	5
2.The linear program organizations using Assembler-86	2		2	5	5
3.The branched and cyclic programs organization using Assembler-86 language	14		4	5	5
1 module in total, h.	18	–	8	15	15

The content of substantial modules (lecture hours - 18):

2.1 Programming language Assembler-86 (2 h.)
The content: Low-level programming languages. Assembly programming language. Instruction and data formats. Operand addressing modes. Move instructions.

2.2 The linear program organisation using Assembly language (2 h.)
The content: Data conversion instruction in Assembly language. The linear programs.

2.3 The branched and cyclic programs organisation using Assembly language
The content: Conditional and unconditional jump instructions in Assembly language. The branched programs.; The organisation of cyclic programs.; Data exchange modes in MPS. The user interface software in typical MPS.; Organization of interrupts in MPS. Types of interrupts.; Productivity of microprocessors and estimation of it. Architecture of modern microprocessors.; Intel microprocessors using in telecommunication. Software support of telecommunications facilities nodes.

Laboratory studies' themes of the module 2

№	NUMBER, THE NAME OF LABORATORY WORKS	Hours
1	The linear programs	2
2	The branched programs	2
3	The cyclic programs	2
4	Serial port RS-232-C	2
	In total	8

Initial knowledge and abilities from the module 2

№	The content of knowledge	The code number
1	To know the operand addressing modes, move instructions, conditional and unconditional jump instructions, organisation interrupts in MPS .	KN.1
2	To know the software support of telecommunications facilities nodes.	KN.2
	The content of abilities	
1	To put and solve the problems connected with the analysis, working out and operation of different functional MPS, creation and software debugging of them.	AB.1
2	To analyze and develop separate telecommunications systems nodes which use computer means and microprocessors. To use typical digital blocks, nodes and elements for digital devices realization.	AB.2
3	To put and solve the problems connected with a computer means choice, microprocessors behind their technical, operational and economic characteristics for systems of telecommunications.	AB.3

The module 3: Microprocessor systems (MPS) on universal microprocessors and its programming

Entrance requirements to module studying (knowledge and ability from disciplines which provide studying of the given module).

№	The content of knowledge	The code number
1	The general MPS architecture	KN.1
2	Microprocessors programming bases	KN.2
	The content of abilities	
1	Communication networks designing	AB.1
2	Communication networks tumimg	AB.2

Structure of the test module 3

The substantial module	Lecture (hours)	Employment		Self-instruction	Individual work
		practical	laboratory		
The module 3: Microprocessor systems (MPS) on universal microprocessors and its programming (2 credits; 52 ч.)					
1. x-bit Motorola microprocessors	4		2	4	4
2. MPS construction on 32-bit Motorola MP	6		2	5	5
3. MPS software creation on 32-bit Motorola MP	6		4	5	5
1 module in total, h.	16	–	8	14	14

The content of substantial modules (lecture hours - 16):

3.1 x-bit Motorola microprocessors (4 h.)
The content: Motorola MP MC68XXX. Software models of MP MC68000 and 68020.; Memory organisation and operand addressing modes in MP MC68XXX.

3.2 MPS construction on 32-bit Motorola MP (6 h.)
The content: Principles of MPS construction on MP MC68XXX.; Distribution of address space in MPS on MP MC68XXX. The organisation of a memory subsystem.; The organisation of a peripheral subsystem.

3.3 Creation of the software for MPS on 32-bit Motorola MP (6 ч.)
The content: Instruction set of MP MC68000. Examples of programs with different operand addressing modes in instructions.; Control transfer instruction in MP MC68XXX.; Construction of programs with structure "branching" and "cycle" in MP MC68XXX.

Laboratory studies' themes of the module 3

№	NUMBER, THE NAME OF LABORATORY WORKS	Hours
1	Monitor instructions studying of Motorola MC 68xxx	2
2	Structure and operand addressing modes of typical instructions in Motorola MP 68xxx	2
3	Instruction set of Motorola MP 68xxx	2
4	Programming of Motorola MP 68xxx	2
	In total	8

Initial knowledge and abilities from the module 3

№	The content of knowledge	The code number
1	To know the structure and addressing modes in typical commands of Motorola MP 68xxx.	KN.1
2	MPS construction principles. Memory subsystem organisation. Peripheral subsystem organisation.	KN.2
	The content of abilities	
1	To put and solve the problems connected with the analysis, working out and microprocessor systems operation of different function, creation of the software debugging them.	AB.1
2	To analyze and develop separate telecommunications systems nodes which use computer aids, microprocessors and microcontrollers. To use typical digital blocks, nodes and elements for digital devices realization.	AB.2

The module 4: Microprocessor systems on microcontrollers and DSP and its programming.

Entrance requirements to module studying (knowledge and ability from disciplines which provide studying of the given module).

№	The content of knowledge	The code number
1	General MPS architecture	KN.1
2	Microprocessors programming bases	KN.2
	The content of abilities	
1	Communication networks designing	AB.1
2	Communication networks tumimg	AB.2

Structure of the test module 4

The substantial module	Lecture (hours)	Employment		Self-instruction	Individual work
		practical	laboratory		
The module 4: Microprocessor systems on microcontrollers and DSP and its programming (1 credit; 56 h.)					
1. Motorola microcontrollers	4		2	2	2
2. MPS construction on Motorola MC	4		2	3	3
3. Software creation for MPS on Motorola MC	6		2	5	5
4. Digital signals processors	4		2	5	5
1 module in total, h.	18	–	8	15	15

The content of substantial modules (lecture hours - 16):

4.1 Motorola microcontrollers (4 h.)
The content: Motorola Microcontrollers (MC): HC05, HC08, HC11. Structure; MC intrinsics.

4.2 MPS construction on Motorola MC (4 h.)
The content: Adjustment of the MC intrinsics.; Typical MC programming examples.

4.3 Software creation for MPS on Motorola MC (6 h.)
The content: Motorola RISC-processors; General principles of the digital signals processing.; Construction principles of telecommunications nodes at program level .

4.4 Digital signals processors (4 h.)
The content: Architecture and construction principles of digital processors (DSP), its features and field of use.; Microprocessor systems in terms of the DSP, universal MP and MC.

Laboratory studies' themes of the module 4

№	NUMBER, THE NAME OF LABORATORY WORKS	Hours
1	The organisation branched programs in Motorola MP 68xxx using Assembly language	2
2	The organisation cyclic programs in Motorola MP 68xxx using Assembly language	2
3	Instruction set of Motorola 68HC05microcontroller	2
4	Motorola 68HC05 microcontroller processor module and technological features structure studying.	2
	In total	8

Initial knowledge and abilities from the module 4

№	The content of knowledge	The code number
1	To know Instruction set of the Motorola 68HC05 microcontroller, processor module structure and technological features of the microcontroller.	KN.1
	The content of abilities	
1	To put and solve the problems connected with a computer aids choice, microprocessors and microcontrollers behind its technical, operational and economic characteristics for telecommunications systems.	AB.1
2	To create and adjust the software for digital signals processing devices in telecommunications systems using languages of specific microprocessors and microcontrollers.	AB.2
3	To submit and treat entrance and initial numerical data for the further digital processing. To correlate logic changes and functions to digital signals which realize its.	AB.3

1. Study objective

The acquaintance with construction principles and schemes of memories in microprocessor systems.

2. Key points

2.1. Storage devices

The storage device or just *M* (*Memory*) is one of the basic components of the microprocessor systems, generally, in all the consecutive digital systems where data from present time is transmitted in the future. Such property defines dependence of system outputs not only on inputs, but also on its previous condition that provides practically unlimited ability of transmission of the information.

The data is stored in the memory device by the established portions (words) in the form of figures, letters or symbols. The information word usually consists of eight binary (zero and one) positions, bits (*B1T*) and is called as byte (BY). Each byte of the information takes places in a memory cell (MC), the MC made of eight memory elements (ME), having two steady states: logic zero and unit (*L*0, *L*1). For storage structure the set same numbered MC is characteristic, number of everyone MC is called as its address (*A-address*). Transfer and placing of an information word to the storage to the certain address is called as writing (*WR – write*), delivery of a word from the storage – reading (*RD – read*). At record the former information in MC is automatically erased, at reading – remains invariable. The reference to memory for record or reading usually is called as sample or access.

Structurally various storages share on two basic types: random access memory and serial access memory. In the storage of the first type access to any cell for record or reading occurs for the same time; in the storage of the second type access time variously also depends on an order of placing of words in memory.

2.2. Random-access memory

Random access memory with reading and recording is called as an operative memory (OM) more often, however in techniques other designation is used: *RAM* (*random access memory*). The signal organisation of the typical RAM is presented on fig. 2.1. The address necessary for sample MC is established on the RAM input binary by means of the address bus (BA – *bus address)*, quantity of BA lines is the length of the address or word length depends on capacity of the STORAGE, its quantity MC: $K=2^n$, where K – number of MC, N - number of BA lines. So, for example, the 16 cells RAM capacity demands for sample of every MC of all 4-bit BA: addresses from 0000 to 1111 in a binary notation (0-15); for the RAM of 256

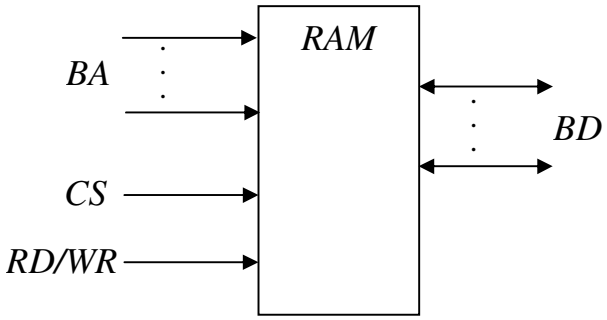

Figure 2.1 – Signal organisation of RAM

cells it is necessary already 8-bit BA: 00000000-11111111 (0-255 addresses, and for the RAM on 65536 cells – 16-bit).

Writing and reading of words in the RAM are usually carried out by means of - the general 8-bit two-forked bus data (*BD*). The RAM Operating mode is set by operating signal (*COWR – control write*): at individual value of signal (high potential) there is a data recording in the RAM, at zero (low potential) – reading. In case of need the RAM can be at all disconnected from BD. One more operating signal is for this purpose applied: a choice of the module, microcircuit (choice section *CS*). At zero value of signal CS all outputs of the RAM are established in high-impedance condition *Z* and do not load BD, being disconnected from it.

Switching-off of the RAM from BD is widely used at block or section construction of memory. On fig. 2.2 as an example the structure of the storage capacity of 256 cells, consisting of 16 separate blocks on 16 cells is shown. All blocks of the storage (SD0-SD15) are included in parallel on the general BD, and by means of the special decoder (DC) only one block is chose. DC work is controlled by the high half-byte of the address (categories 8-15, all the category here are numbered as a seniority). Depending on an entrance combination of the high half-byte, DC raises one target bus and by means of signal BA connects to BD one block of memory. In the chosen block in low half-byte addresses (categories 4-1) the required cell of memory is defined. At construction of schemes MD it is applied as well expansion of the digits per words. On fig. 2.3 parallel switching on BA and consecutive on BD two 4-bit storages is shown, as a result the length of a word on BD doubles.

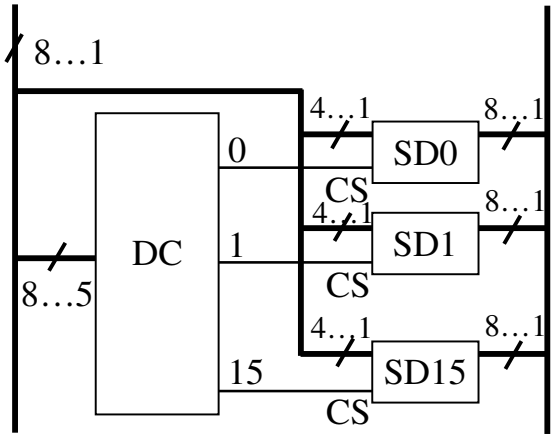

Figure 2.2 – Structure of the storage device

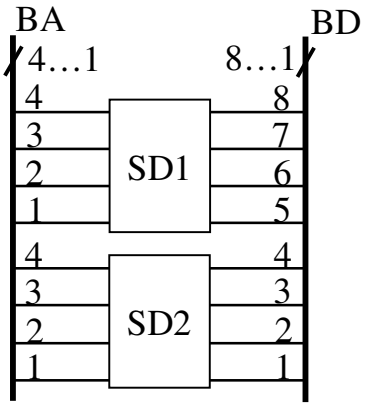

Figure 2.3 – Connection of two 4-bit storage devices

The typical block-diagram of the RAM is presented on fig. 2.4.

The information of MC address the RAM in a binary *N*-bit code on BA moves on an input of the decoder of address (DCA). Depending on an entrance combination of units and zero, DCA raises, establishes logic unit on one of the 2^N output buses. Raised output bus DCA as initiates an address line for record or reading one MC, consisting of eight low case ME. Located by column various MC form the categories of words with the same name on BD (8-1), the operating mode of everyone ME is established by general bus. Such design of the RAM provides possibility for an identical interval of time by means of an address line to carry out sample any MC for record or reading of one byte of the data. For example, at *N*=4 for 1010 address on the tenth line DCA it is established logic unit (high potential) and to BD eight are connected for record or reading digit ME by the tenth MC. At low level of signal all block of the RAM is disconnected from CS, in this

case on all outputs DCA (address lines of the storage) the low potential set up and all MC are disconnected from BD.

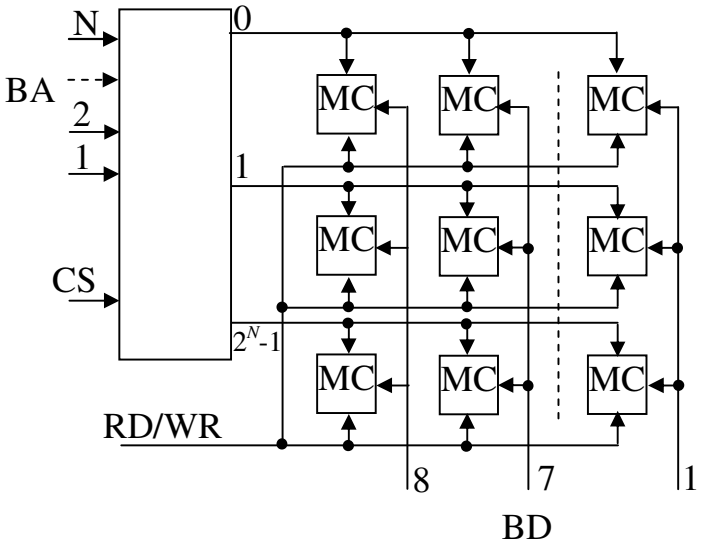

Figure 2.4 – Structure chart of RAM

One of possible circuit realisations ME RAM is shown on fig. 2.5. Basis ME is made by the RS-trigger, the T-device with two steady conditions. While setting on a R-input of the trigger logic unit on its output the logic zero is adjusted, at giving on a S-input

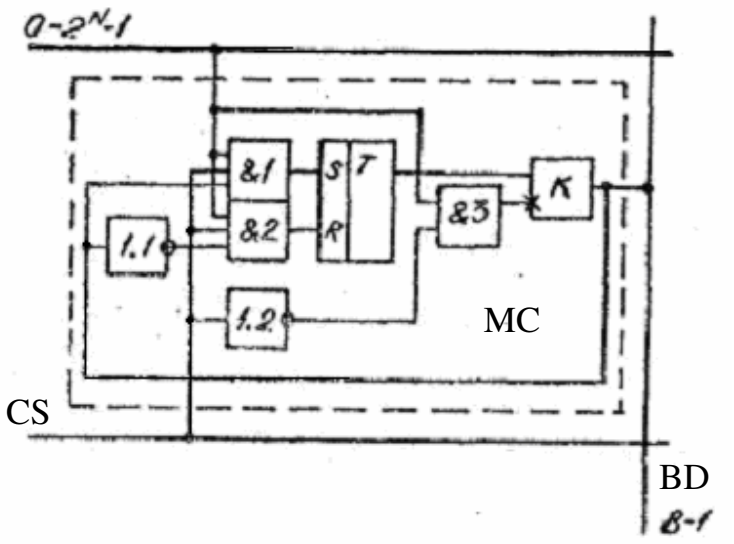

Figure 2.4 – Realisation MC of RAM

of logic unit on a trigger exit logic unit is adjusted also: *R* - dump (*reset*), *S* installation (*set*). Three switching elements are included in scheme ME and, designated as and (And - the element of logic multiplication or coincidence, on its exit is established logic unit only at giving of logic units on all its inputs), two inverters 1 and 2 (on an inverter exit - a signal

opposite to the input), and also a three-stable key element K (*SW - switch*) also. At an individual signal on an operating input the key element spends an entrance signal in the form of logic zero and units on the output, at zero - does not spend (the third condition), sets an exit in high-impedance a condition and being disconnected from loading, BD.

In a record mode on line rec the signal of high level is established (logic unit), the inverter 2 gives out logic zero on one input of an element AND 3, on an output AND logic zero formed and a key element K disconnected from BD. After that on BD the information for record in the RAM from the output moves, at record of unit element AND 1 spends logic unit to trigger T *S-input* and forms it in an individual condition on the output. At zero record element AND 2 joins and, influencing a trigger *R-input*, sets on its output logic zero. The information written down in the trigger remains all time of giving of power supplies for the RAM and is erased only at repeated record. In a mode of reading a signal on line rec of low level (logic zero), element AND 1 and AND 2 are closed, and AND 3 opens, connecting by means of a key element K an output of trigger T with BD, sending thus on BD the information of the condition, former record.

As it was specified, the condition of trigger T and, hence, information ME is lost at power supplies switching-off, therefore all types of the RAM are volatile. The RAMs storing the information all time of giving of power supplies, are called static. There are also dynamic RAMs (*RAMD*), keeping the information at included power supplies very short time, some milliseconds, and to a stream updating demanding additional special devices, regeneration the data. Dynamic RAMs are characteristic more simple scheme MC, hence, greater in capacity, and also is considerable smaller power consumption, therefore have certain advantages before the static.

2.3. Read only memory

In many practical cases are necessary for the storage with the invariable information, for example, for storage of the list of constants, tables of symbols, constant programs of work of mps, etc. For these purposes the constant memories designated by symbol *ROM* (*read only memory*) are applied. ROM application gives notable advantages in front of the RAM: ROM are non-volatile, their information does not collapse at power supply de-energization, besides, MC ROM architecturally are very simple, that gives the chance to raise considerably its capacity on the standard area of a crystal.

ROM block diagramme is shown on fig. 2.6. Here it is similar to the RAM scheme an address binary combination on BA raises one exit DCA - a line of the address. The constant information of a word is formed every line on BD digit-by-digit by means of specially chosen switching of inputs of elements OR 1 (a collective element OR, the element of logic addition establishes logic unit on the output at occurrence at least one logic unit on inputs). So, for example, at excitation of a zero address line of ROM (00 address... 0) on BD there will be a word 10... 1 as by this line inputs of elements OR 1.8 and 1.1 are connected. At excitation of the first line (00 address... I) on BD there will be a word 01 … 1, and to high 11 address... 1 (a line 2^N-I) the word 11 … 0 is written down. In ROM with operating signal CS it is necessary to apply three-stable elements OR, passing in a mode of

high-impedance *Z* at low level of signal CS (on fig. 2.6 line of signal BM is not shown).

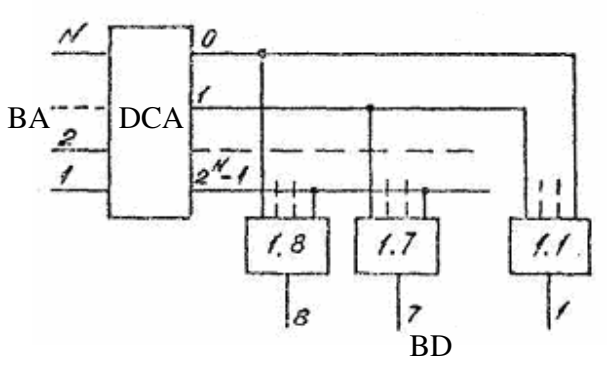

Figure 2.6 – Structure chart of RAM

The basic scheme of ROM is simple enough (fig. 2.7). Here it is applied DCA with inverse exits 0 … 2^N-I (on raised exit DCA the low potential is set up), digit lines of columns BD through restrictive resistors *R* are connected to a source of pressure *E*, and between address lines DCA and digit lines of columns, depending on the information of words of ROM, by means of crosspieces P diodes *D* playing a role of inputs of elements OR are included. Inverse outputs DCA are necessary for switching-off of diodes on not chosen address lines.

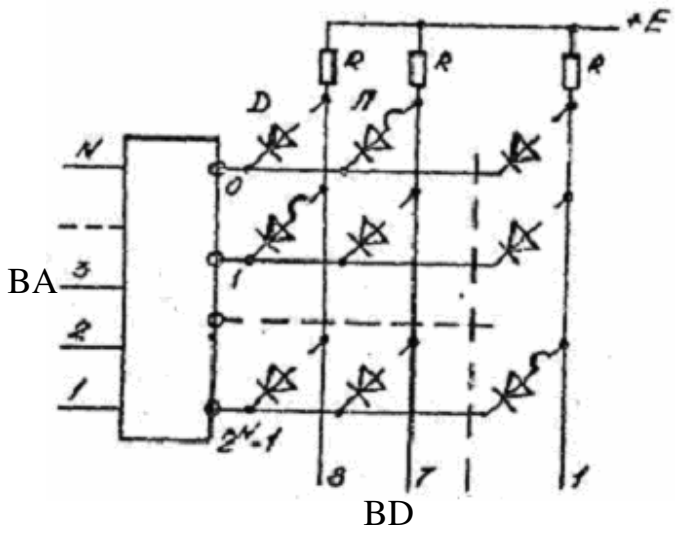

Figure 2.7 – Basic scheme of ROM

At excitation, for example, a zero line DCA (00 address... 0) its potential become low, therefore on lines of the columns connected with raised line by diode *D* and crosspiece P, will be established also low potential, and after inverting - high: on BD to 00 address... 0 there will be a word 10... 1. Similarly to 00 address... 1 corresponding installation of

crosspieces writes down a word 01... 1, and to 11 address... 1 - a word 11... 0. In need of introduction in ROM of signal CS on BD three-stable elements are established.

2.4. Programmable read-only memory

The data recording in ROM is made by manufacturer a dusting of necessary crosspieces by means of a special mask, and further these data cannot be changed. Such ROM is economically profitable only at mass consumption and a large-lot production. However in some cases it is expedient to write down the necessary information in ROM individually and directly at the consumer. For this purpose in a matrix of ROM the manufacturer establishes all fusible crosspieces, and by means of special programmer unnecessary crosspieces collapse, fused by short-term giving of the forced supply. Such constant memories unitary programmed by the consumer constant MD, designated as *PROM* (*programmable read only memory*) have received a wide circulation.

In some cases while in service it is necessary to change information constant MD, therefore are applied and reprogrammed constant MD *RPROM* (*reprogrammable read only memory*). Usually RPROM are designed with use of effect of a charge of the capacitor of the isolated "floating" gate finger of the special MOS-transistor. High isolation of a "floating" gate finger allows to keep a charge of its capacitor enough the big term - some years, if necessary this charge can be removed ultra-violet radiation, i.e. to "erase" all information RPROM. Installation of a charge of the condenser of a gate finger of the MOS-transistor is made for record of the new information by means of short-term breakdown of an interval a drain-shutter by the forced pressure of a supply.

3. Control questions

3.1 Why is the BA of the RAM unidirectional and the BD bi-directional?
3.2 How the BA capacity of the storage device is defined?
3.3 For what purpose does operating signal CS serve in the storage?
3.4 How the capacity and word length of the storage are increased?
3.5 What appointment of trigger T in scheme MC in the RAM is?
3.6 For what purpose is three-stable key element K entered in scheme MC in the RAM?
3.7 What a difference is between static and dynamic RAMs?
3.8 What a difference is between RAM and ROM?
3.9 What role do the diodes and jumpers have in ROM scheme?
3.10 Is it possible to enter operating signal CS into ROM scheme?
3.11 Is it possible to change data in the PROM?

4. Homework

To give answers to control questions.

5. Laboratory task

5.1 Acquaint with laboratory equipment using item 6.
5.2 Read and write down into table data of all addresses for the ROM.
5.3 Overwrite all information from ROM into RAM.
5.4 Enter into the RAM in the cells, specified by the teacher, the set new words.

6. Laboratory equipment

On a laboratory breadboard the simplified scheme of the 8-bit storage block with capacity in 16 cells (words) is shown.

The basic nodes of the laboratory breadboard:

- the patch board of 4 buttons and status indicators for a low half-byte choice of BA address, bits 4P-1P (“Адрес”);
- the patch board of 8 buttons for data input into BD, bits 8P-1P (“Данные”);
- the patch board of 5 buttons for control of the storage device work;
  „Выбор ЗУ” – switching on the decoder for a storage block choice;
  „Данные” – data input into BD;
  „Зп ОЗУ” – data writing from BD into RAM to the set address;
  „Сч ОЗУ” – data reading from RAM into BD to the set address;
  „Сч ПЗУ” – data reading from ROM into BD to the set address,
- information indicator of 8-bit word on BD (“Шина данных”);
- decoder for a storage block choice of 16 storage blocks (БЗУ0-БЗУ15), the high half-byte (8P-5P bits) of 8-bit BA address equals to zero (0000);
- two modules of 4-bit RAM;
- module of 8-bit ROM.

7. Contents of the protocol

It is necessary to record the title and purpose of the laboratory work, to prepare homework, to represent the block diagram of the laboratory breadboard and laboratory work execution results.

8. The literature list

8.1 Бедрековский М.А., Кручинкин Н.С., Подолян В.А. Микропроцессоры. – М.: Радио и связь, 1981. - 70 с.

8.2 Балашов Е.П., Пузанков Д.В. Микропроцессоры и микропроцессорные системы. – М.: Радио и связь, 1981. - 326 с.