Ministry of Transport and Communications of Ukraine

State Administration of Communications of Ukraine

Odessa National Academy of Telecommunications after A.S. Popov

Department of Computer Science and Microprocessors

Computer Science and Microprocessors

Module №1

Units of computer facilities and microprocessor systems

for students

ARITHMETIC LOGIC UNIT

training area: telecommunications

for specialties: 7. 092402, 7. 092401, 7. 092404, 7. 092407

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Writer: Tkachenko A.A.

The organisation of the arithmetic logic units (ALU) is considered. The most used modern structure of the ALU is chosen for laboratory research. The scheme and the description of laboratory installation, variants of tasks and order of the laboratory work execution are presented.

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I. Foreword

Discipline general characteristic (quantity of credits ECTS - 6; modules - 4; substantial modules - 14; total hours - 216; including: lectures - 68 h.; laboratory works - 32 h.; practical trainings - 0 h.; independent work - 58 h.; individual work - 58 h.; semester 2.3, 2.4, 3.1, 3.2, a control kind: the complex task, the course work, the test.

II. The purpose of discipline training

The purpose and subject matter of problems: knowledge formation concerning computer aids construction principles and microprocessor systems, creation and software debugging of them, ability to analyse, working out and operate such systems in telecommunications.

III. The discipline content

Electronic computers nodes of: digital automatic machines, both their analysis and synthesis; memory devices, their classification and the organization; microprocessors (MP), construction principles and microprocessors and electronic computers functioning, universal microprocessors architecture, the organisation of memory and ways of addressing of operands in microprocessors.

Microprocessor systems (MPS): construction principles, ways of the organisation of data exchange in MPS, address space and its distribution in MPS, typical user MPS interface hardware and program means, the interruptions organisation in MPS; controllers in telecommunications, microcontrollers of conducting firms, control means and switching construction in systems of telecommunications at hardware and program levels; digital signals processors in telecommunications, conducting firms digital signals processors, telecommunications systems signals transformation modules construction on hardware and program levels; MPS productivity increase , multiprocessing system.

The MPS software: programming of MT INTEL firm, the raised word length MT programming of conducting firms; microcontrollers and processors digital signals programming.

The module 1: Units of computer facilities and microprocessor systems

Entrance requirements to module studying (knowledge and abilities from disciplines which provide studying of the given module).

№	The content of knowledge	The code number
1	Number representations	KN.1
2	Circuitry bases	KN.2
	The content of abilities	
1	Designing of communication networks	AB.1
2	Communication networks tumimg	AB.2

Structure of the test module 1

The substantial module	Lecture (hours)	Study		Self-instruction	Individual work
		practical	laboratory		
The module 1: The nodes of computer facilities and microprocessor systems (2 credits; 52 h.)					
1. Computer aids	4		2	2	2
2. Microprocessors	6		2	4	4
3. Memory subsystems	4		2	4	4
4. Interfaces	2		2	4	4
1 module in total, h.	16	–	8	14	14

The content of substantial modules (lecture hours - 16):

1.1 Computer aids (4 h.)

The content: Computer and microprocessor systems.; Data manipulation in computer systems.

1.2 Microprocessors (6 h.)

The content: Digital automaton. Digital automata synthesis.; Typical computer systems devices.; Microprocessors architecture. Software models of the 16- and 32-bit Intel microprocessors.

1.3 Memory subsystems (4 h.)

The content: Memory construction principles with the set organization.; Address space and its distribution in MPS. Memory segmentation. Operand addressing modes for the Intel microprocessors.

1.4 Interfaces (2 h.)

The content: Principles of the computer construction and its functioning. Interfaces.

Laboratory studies' themes of the module 1

№	NUMBER, THE NAME OF LABORATORY WORKS	Hours
1	Arithmetic logic unit	2
2	Storage device	2
3	Architecture and software models of Intel microprocessors	2
4	Memory segmentation	2
	In total	8

Initial knowledge and abilities from the module 1

№	The content of knowledge	The code number
1	To know the construction principles of arithmetic logic and memory devices	KN.1
2	To know architecture and operand addressing modes for the Intel microprocessors.	KN.2
	The content of abilities	
1	To submit and treat entrance and initial numerical data for the further digital processing. To correlate logic changes and functions to digital signals which realize them.	AB.1
2	To put and solve the problems connected with the analysis, working out and operation of microprocessor systems of different function, creation and to software debugging to them.	AB.2

The module 2: Programming of Intel microprocessors .

Entrance requirements to module studying (knowledge and abilities from disciplines which provide studying of the given module).

№	The content of knowledge	The code number
1	Number representations	KN.1
2	Circuitry bases	KN.2
3	The general principles of programming	KN.3
	The content of abilities	
1	Designing of communication networks	AB.1
2	Communication networks tumimg	AB.2

Structure of the test module 2

The substantial module	Lecture (hours)	Employment		Self-instruction	Individual work
		practical	laboratory		
The module 2: Intel microprocessors programming (1 credit; 56 ч.)					
1. Programming language Assembler-86	2		2	5	5
2. The linear program organizations using Assembler-86 language	2		2	5	5
3. The branched and cyclic programs organization using Assembler-86 language	14		4	5	5
1 module in total, h.	18	–	8	15	15

The content of substantial modules (lecture hours - 18):

2.1 Programming language Assembler-86 (2 h.)
   The content: Low-level programming languages. Assembly programming language. Instruction and data formats. Operand addressing modes. Move instructions.

2.2 The linear program organisation using Assembly language (2 h.)
   The content: Data conversion instruction in Assembly language. The linear programs.

2.3 The branched and cyclic programs organisation using Assembly language
   The content: Conditional and unconditional jump instructions in Assembly language. The branched programs.; The organisation of cyclic programs.; Data exchange modes in MPS. The user interface software in typical MPS.; Organization of interrupts in MPS. Types of interrupts.; Productivity of microprocessors and estimation of it. Architecture of modern microprocessors.; Intel microprocessors using in telecommunication. Software support of telecommunications facilities nodes.

Laboratory studies' themes of the module 2

№	NUMBER, THE NAME OF LABORATORY WORKS	Hours
1	The linear programs	2
2	The branched programs	2
3	The cyclic programs	2
4	Serial port RS-232-C	2
	In total	8

Initial knowledge and abilities from the module 2

№	The content of knowledge	The code number
1	To know the operand addressing modes, move instructions, conditional and unconditional jump instructions, organisation interrupts in MPS .	KN.1
2	To know the software support of telecommunications facilities nodes.	KN.2
	The content of abilities	
1	To put and solve the problems connected with the analysis, working out and operation of different functional MPS, creation and software debugging of them.	AB.1
2	To analyze and develop separate telecommunications systems nodes which use computer means and microprocessors. To use typical digital blocks, nodes and elements for digital devices realization.	AB.2
3	To put and solve the problems connected with a computer means choice, microprocessors behind their technical, operational and economic characteristics for systems of telecommunications.	AB.3

The module 3: Microprocessor systems (MPS) on universal microprocessors and its programming

Entrance requirements to module studying (knowledge and ability from disciplines which provide studying of the given module).

№	The content of knowledge	The code number
1	The general MPS architecture	KN.1
2	Microprocessors programming bases	KN.2
	The content of abilities	
1	Communication networks designing	AB.1
2	Communication networks tumimg	AB.2

Structure of the test module 3

The substantial module	Lecture (hours)	Employment		Self-instruction	Individual work
		practical	laboratory		
The module 3: Microprocessor systems (MPS) on universal microprocessors and its programming (2 credits; 52 ч.)					
1. x-bit Motorola microprocessors	4		2	4	4
2. MPS construction on 32-bit Motorola MP	6		2	5	5
3. MPS software creation on 32-bit Motorola MP	6		4	5	5
1 module in total, h.	16	–	8	14	14

The content of substantial modules (lecture hours - 16):

3.1 x-bit Motorola microprocessors (4 h.)
   The content: Motorola MP MC68XXX. Software models of MP MC68000 and 68020.; Memory organisation and operand addressing modes in MP MC68XXX .

3.2 MPS construction on 32-bit Motorola MP (6 h.)
   The content: Principles of MPS construction on MP MC68XXX.; Distribution of address space in MPS on MP MC68XXX. The organisation of a memory subsystem.; The organisation of a peripheral subsystem.

3.3 Creation of the software for MPS on 32-bit Motorola MP (6 ч.)
   The content: Instruction set of MP MC68000. Examples of programs with different operand addressing modes in instructions.; Control transfer instruction in MP MC68XXX.; Construction of programs with structure "branching" and "cycle" in MP MC68XXX.

Laboratory studies' themes of the module 3

№	NUMBER, THE NAME OF LABORATORY WORKS	Hours
1	Monitor instructions studying of Motorola MC 68xxx	2
2	Structure and operand addressing modes of typical instructions in Motorola MP 68xxx	2
3	Instruction set of Motorola MP 68xxx	2
4	Programming of Motorola MP 68xxx	2
	In total	8

Initial knowledge and abilities from the module 3

№	The content of knowledge	The code number
1	To know the structure and addressing modes in typical commands of Motorola MP 68xxx.	KN.1
2	MPS construction principles. Memory subsystem organisation. Peripheral subsystem organisation.	KN.2
	The content of abilities	
1	To put and solve the problems connected with the analysis, working out and microprocessor systems operation of different function, creation of the software debugging them.	AB.1
2	To analyze and develop separate telecommunications systems nodes which use computer aids, microprocessors and microcontrollers. To use typical digital blocks, nodes and elements for digital devices realization.	AB.2

The module 4: Microprocessor systems on microcontrollers and DSP and its programming.

Entrance requirements to module studying (knowledge and ability from disciplines which provide studying of the given module).

№	The content of knowledge	The code number
1	General MPS architecture	KN.1
2	Microprocessors programming bases	KN.2
	The content of abilities	
1	Communication networks designing	AB.1
2	Communication networks tumimg	AB.2

Structure of the test module 4

The substantial module	Lecture (hours)	Employment		Self-instruction	Individual work
		practical	laboratory		
The module 4: Microprocessor systems on microcontrollers and DSP and its programming (1 credit; 56 h.)					
1. Motorola microcontrollers	4		2	2	2
2. MPS construction on Motorola MC	4		2	3	3
3. Software creation for MPS on Motorola MC	6		2	5	5
4. Digital signals processors	4		2	5	5
1 module in total, h.	18	–	8	15	15

The content of substantial modules (lecture hours - 16):
4.1 Motorola microcontrollers (4 h.)
   The content: Motorola Microcontrollers (MC): HC05, HC08, HC11. Structure; MC intrinsics.
4.2 MPS construction on Motorola MC (4 h.)
   The content: Adjustment of the MC intrinsics.; Typical MC programming examples.
4.3 Software creation for MPS on Motorola MC (6 h.)
   The content: Motorola RISC-processors; General principles of the digital signals processing.; Construction principles of telecommunications nodes at program level .
4.4 Digital signals processors (4 h.)
   The content: Architecture and construction principles of digital processors (DSP), its features and field of use.; Microprocessor systems in terms of the DSP, universal MP and MC.

Laboratory studies' themes of the module 4

№	NUMBER, THE NAME OF LABORATORY WORKS	Hours
1	The organisation branched programs in Motorola MP 68xxx using Assembly language	2
2	The organisation cyclic programs in Motorola MP 68xxx using Assembly language	2
3	Instruction set of Motorola 68HC05microcontroller	2
4	Motorola 68HC05 microcontroller processor module and technological features structure studying.	2
	In total	8

Initial knowledge and abilities from the module 4

№	The content of knowledge	The code number
1	To know Instruction set of the Motorola 68HC05 microcontroller, processor module structure and technological features of the microcontroller.	KN.1
	The content of abilities	
1	To put and solve the problems connected with a computer aids choice, microprocessors and microcontrollers behind its technical, operational and economic characteristics for telecommunications systems.	AB.1
2	To create and adjust the software for digital signals processing devices in telecommunications systems using languages of specific microprocessors and microcontrollers.	AB.2
3	To submit and treat entrance and initial numerical data for the further digital processing. To correlate logic changes and functions to digital signals which realize its.	AB.3

1. Study objective

The acquaintance with the structural organisation of the microprocessors' (MP) arithmetic logic unit (ALU) and research of its functionality.

2. Key points

The ALU serves for performing arithmetic, logic and bit-shifting operand operations. Generally, the ALU is the multifunction device in which such operations are carried out:

Binary arithmetic operations with the fixed-point numbers;

Binary (or hexadecimal) arithmetic operations with the floating-point numbers;

Decimal arithmetic operations;

Index arithmetic operations (by updating commands' addresses);

Special arithmetic operations;

Logic operations;

Operations with the logic operands.

By the way of action with operands ALU is divided into sequential and parallel. In the sequential ALU operand operations are carried out in time bit-by-bit. In the parallel ALU operand operations are carried out parallel-by-bit.

By the way of number representation ALU is divided:

For the fixed-point numbers;

For the floating-point numbers;

For decimal numbers.

By the kind of elements' using ALU is divided into block and multipurpose.

In modern MP ALUs' mostly are used operational units (in the sequel ALU) of combinational type.

The majority of carried out operations in ALU require two operands stored in two registers – Rg1 and Rg2. In the first models of ALU the principle of accumulator "bottleneck" (fig.2.1,a) when one of operands stored in the fixed register-accumulator A where the result of the operation was sent was used. Such operations require in single-address commands (in the operands' field of the command – one operand), but thus the program becomes complicated. In later models of ALU have refused the register-accumulator for the benefit of a register file, where each register "the accumulator by itself", (fig.2.1,b), which in general assisted increase of productivity.

In the modern RISC-structures of MP with mainly register addressing use ALU with the structure shown in fig.2.1 [8.3].
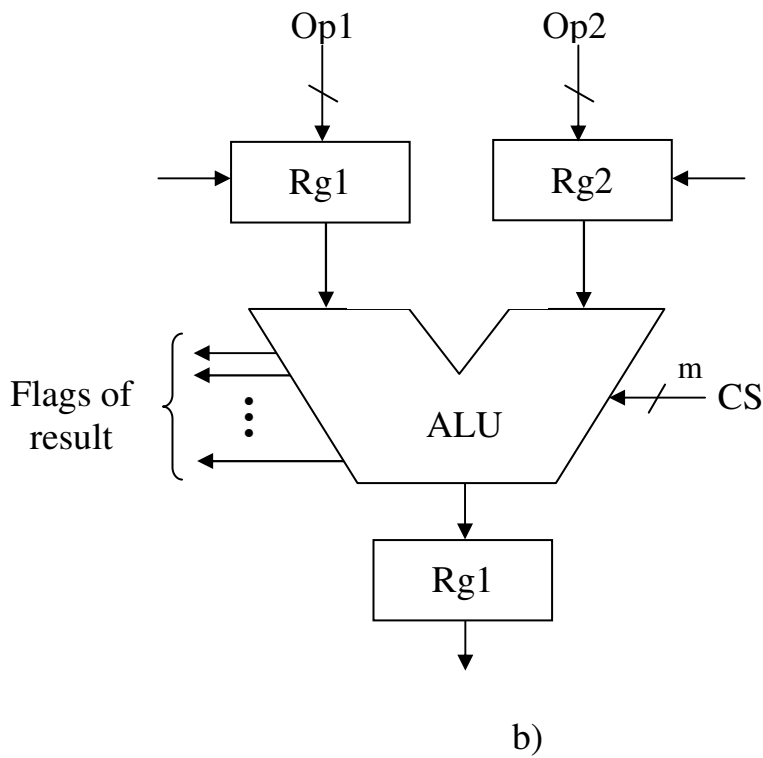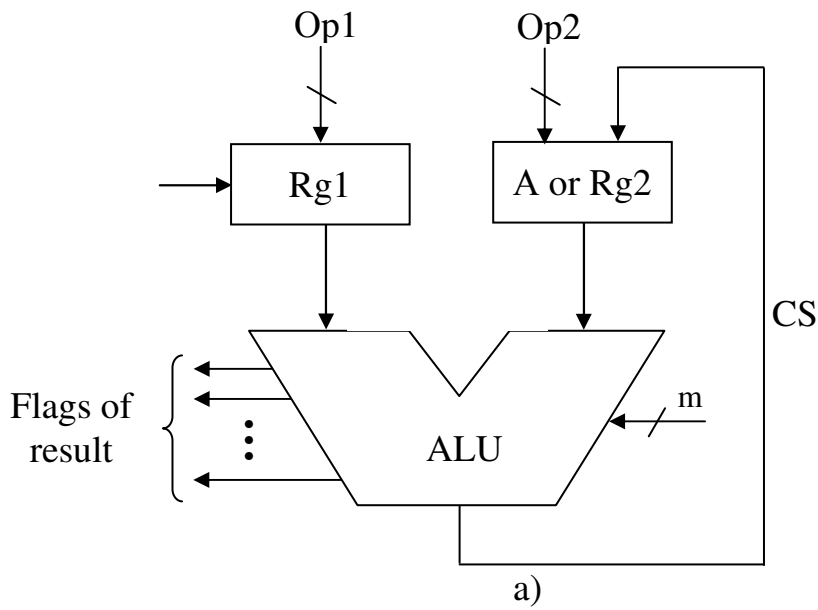
Figure 2.1 – Logical structures of the ALU

Quantity of flags which are formed in ALU and are used in MP depends on type of MP.

Operation in ALU is carried out if there are the control signals (CS) which are formed in general with using of a code of command's operation.

By the functions ALU is the operational device that performs the micro operations which provide receiving of operands from other devices (for example the basic memory), their conversion and transfer of conversion results to other devices.

Together with result in ALU, flag bits of result stored in the flag register F are formed (on fig.2.1 it is not designated).

Maximum quantity of flags – 6:

− zero flag – flag bit gains the level L1, if result amounts to nothing, differently – L0;
− sign flag – flag bit gains the level L1, if result is negative, differently – L0;
− carry flag – flag bit gains the level L1, if there is the carry from high-order bit, differently – L0;
− parity flag – flag bit gains the level L1, if result has even quantity of units, differently – L0;
− overflow flag – flag bit gains the level L1, if there is the overflow of a bit grid;
− auxiliary carry flag – flag bit gains the level L1, if there is the carry from the low tetrad into the high tetrad, differently – L0.

For different families of MP the certain flags are designated variously, therefore above at definition of flags their some designations were not specified.

In multipurpose ALU for all ways of number representation the operations are carried out with the same units which are switched in certain way, according to performance of corresponding operation.

In block ALU operations with the fixed-point and floating-point numbers, decimal numbers and alphanumeric fields are carried out with the separate functional blocks. The parallel work's possibility of the specified blocks and also application in them of conveyors (simultaneous performance of several commands) increase speed of operations' performance in such ALU. But circuits of block ALU are more difficult than multipurpose. Their wide application became possible owing to technological achievements of modern microelectronics and circuitry.

ALU functions when there are the control signals (CS) which are formed in the control device and are defined with a code of command's operation.

In general modern ALU or the separate functional blocks of ALU consist of register set and combinational operational unit ALU (OU ALU) in which operations are carried out. For MP there is a typical structure when internal registers are used and as registers of ALU.

At the programs' performance the first five flags are used in branch instruction. It should be noted that the parity flag is used, as a rule, for definition of the erroneous byte (word) which has been transferred by a two-wire line.

The established overflow flag (L1) stops performance of the main program, as the rule, with the further activation of the subroutine performance which informs the user about a contingency.

The established auxiliary carry flag (L1) initiates a result correcting at performance of operations on the binary-decimal numbers.

3. Control questions

3.1 Give the definition of ALU.

3.2 What operations can be carried out in ALU?

3.3 How is divided ALU by the way of action on operands and what ALU are used in the microprocessor?

3.4 How is divided ALU by the way of number representation?

3.5 How is divided ALU by the kind of elements' and units' using?

3.6 What advantages have the block ALU?

3.7 How is divided ALU by the structural organisation?

3.8 How result's flags which are formed in ALU with the microprocessor are used?

4. Homework

4.1 Find out the purpose of separate elements and circuit nodes using the information adduced in the sections 2 and 6 of study guide and in the lecture summary.

4.2 Prepare for discussion of the questions in the section 3.

4.3 Perform the calculations on two operands (according to your variant in the table 4.1). The operand A is a binary eight-bit equivalent of the number made from two last figures of the student's card number, increased on 25. The operand B is a binary eight-bit equivalent of the number made from two last figures of the student's card number, reversed the order and increased on 25.

For example, student's card number is XXX95.
$A=95+25=120_{10}=0111\ 1000_2$
$B=59+25=84_{10}=0101\ 0100_2$
According to the variant №7:

1) $A \oplus B =$
$$\begin{array}{l} \oplus \quad 0\ 1\ 1\ 1\ 1\ 0\ 0\ 0 \\ \quad\ \ 0\ 1\ 0\ 1\ 0\ 1\ 0\ 0 \\ \hline \quad\ \ 0\ 0\ 1\ 0\ 1\ 1\ 0\ 0 - \text{result} \end{array}$$

The flags of result are $Z=0$, $S=0$, $C=0$, $AC=0$ (Z – zero flag, S – sign flag, C – carry flag , AC – auxiliary carry flag).

2) A-B-1

A-B-1=A(ac)+B(ac)+1(ac)=
$$\begin{array}{l} + \quad 0\ 1\ 1\ 1\ 1\ 0\ 0\ 0 \\ \quad\ \ \ 1\ 0\ 1\ 0\ 1\ 1\ 0\ 0 \\ \hline \quad\ \ \ 0\ 0\ 1\ 0\ 0\ 1\ 0\ 0 - \text{subproduct } A\text{-}B \\ + \\ \quad\ \ \ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1 \\ \hline \quad\ \ \ 0\ 0\ 1\ 0\ 0\ 0\ 1\ 1 - \text{result} \end{array}$$

The flags of result are $Z=0$, $S=0$, $C=1$, $AC=1$.
Checking of calculations: $A-B-1=120-84-1=35$
$$0010\ 0011_2=35_{10}$$
Calculations are performed right.
    4.4 Prepare the report of the laboratory work execution.

Table 4.1 – Tasks variants

№	S3	S2	S1	S0	M=1 Logic operations	M=0 Arithmetic operations	
						C0=1	C0=0
1	0	0	0	0	$\overline{A}$	A	$A+1$
2	0	0	0	1	$\overline{A \vee B}$	$A \vee B$	$(A \vee B)+1$
3	0	0	1	0	$\overline{A} \wedge B$	$A \vee \overline{B}$	$(A \vee \overline{B})+1$
4	0	0	1	1	0	-1	0
5	0	1	0	0	$\overline{A \wedge B}$	$(A \wedge \overline{B})+A$	$(A \wedge \overline{B})+A+1$
6	0	1	0	1	$\overline{B}$	$(A \vee B)+(A \wedge \overline{B})$	$(A \vee B)+(A \wedge \overline{B})+1$
7	0	1	1	0	$A \oplus B$	$A-B-1$	$A-B$
8	0	1	1	1	$A \wedge \overline{B}$	$(A \wedge \overline{B})-1$	$A \wedge \overline{B}$
9	1	0	0	0	$\overline{A} \vee B$	$A+(A \wedge B)$	$A+(A \wedge B)+1$
10	1	0	0	1	$\overline{A \oplus \overline{B}}$	$A+B$	$A+B+1$
11	1	0	1	0	B	$(A \vee \overline{B})+(A \wedge B)$	$(A \vee \overline{B})+(A \wedge B)+1$
12	1	0	1	1	$A \wedge B$	$(A \wedge B)-1$	$A \wedge B$
13	1	1	0	0	-1	A^{*}	$A^{*}+1$
14	1	1	0	1	$A \vee \overline{B}$	$(A \vee B)+A$	$(A \vee B)+A+1$
15	1	1	1	0	$A \vee B$	$(A \vee \overline{B})+A$	$(A \vee \overline{B})+A+1$
16	1	1	1	1	A	$A-1$	A

5. Laboratory task

5.1 To acquaint with work-bench setup. To find out with teacher the plan of the LW execution.

5.2 To set operand A in the switch register SA1…SA8 and to write it into the register RG. Then to set operand B in the switch register SA1…SA8. By the use of switch SA15 and the indicator Q7…Q0 to check up presence of operand A and operand B in the specified registers.

5.3 To research the execution of logic operations. By the use of switches SA9…SA13 to set the combination of control signals according to your variant on inputs S3…S0, M of operational unit ALS. To put down the operation result and the flags of result and to compare with data received at homework performance. To draw a conclusions.

5.4 To research the execution of arithmetic operations.

   5.4.1 To leave the switches SA9…A12 in statu quo ante. By the use of switches SA13 and SA14 to set M=0, C0=1. To put down the operation result and the flags of result and to compare with data received at homework performance. To draw a conclusions.

   5.4.2 To repeat item 5.4.1 but to set C0=0.

6. Laboratory equipment

The laboratory equipment consist of the 8-bit operational unit ALU (ALS), the register of operand A (RG), the mechanical register of operand B on switches SA1…SA8, the switches SA9…SA14, the flags indicator Z, S, C, AC, the indicator of the operands and result, that is switched by the use of SA15.

Writing of operand A occurs by the use of switches SA1…SA8 with further electric overwriting to RG by pressing the button SB1.

Then by the use of switches SA1…SA8 to set operand B.

Combination of control signals, that defines specified operation, is set by the use of switches SA9…SA14.

7. Contents of the protocol

It is necessary to record the title and purpose of the laboratory work, to prepare homework according your variant, to execute the necessary calculations, to represent the structural organisation of ALU that is researched, to answer the control questions.
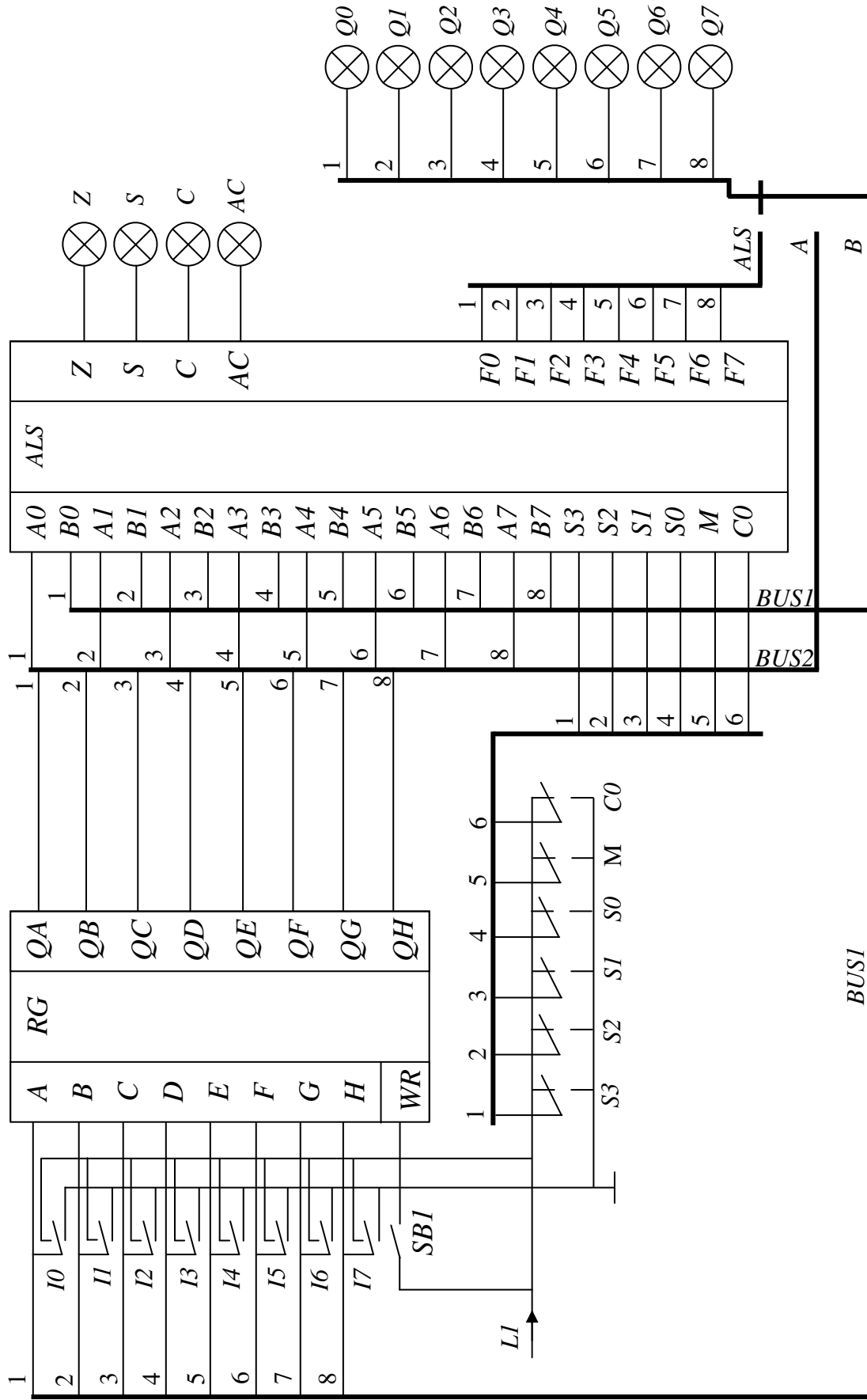
Figure 6.1 – Structure chart of laboratory equipment

8. The literature list

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8.3 Корнеев В.В., Киселев А.В. Современные микропроцессоры. – М.: Нолидж, 1998.